

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
21 December 2000 (21.12.2000)

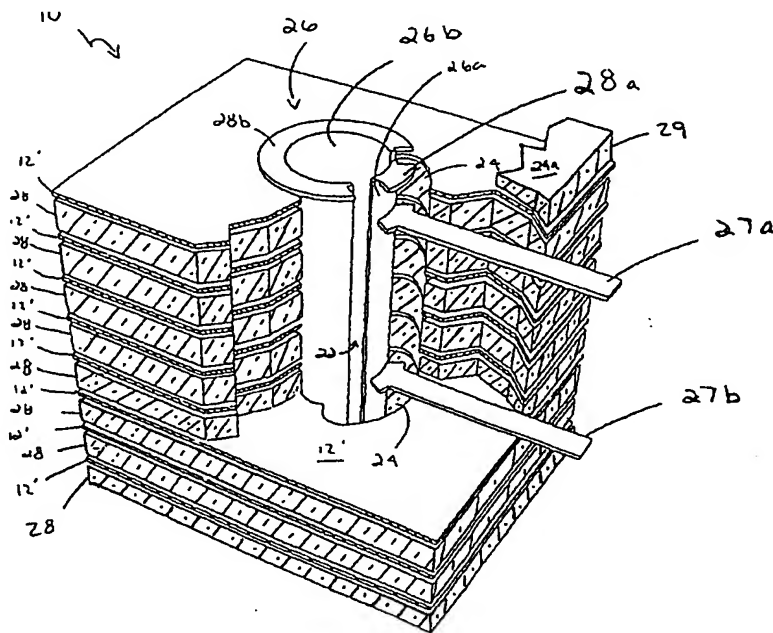
PCT

(10) International Publication Number
WO 00/78105 A1

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- (21) International Application Number: PCT/US00/15551
- (22) International Filing Date: 5 June 2000 (05.06.2000) (74) Agent: DROZENSKI, Diane, C.; Teradyne, Inc., 321 Harrison Avenue, Boston, MA 02118 (US).
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
- | | | |
|------------|---------------------------|----|
| 60/138,730 | 11 June 1999 (11.06.1999) | US |
| 60/139,063 | 11 June 1999 (11.06.1999) | US |
| 60/143,320 | 12 July 1999 (12.07.1999) | US |
| 09/360,002 | 23 July 1999 (23.07.1999) | US |
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- (81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.
- (84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE,

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(54) Title: MULTI-CONNECTION VIA



(57) Abstract: An interconnection circuit and related techniques are described. The interconnection circuit (10) includes a plated through hole (26) having a plurality of electrically isolated segments (26a, 26b) with at least one of the plurality of electrically isolated segments (26a) coupled to a signal path (27a, 27b) and at least one of the electrically isolated segments (26b) coupled to the ground (12). With this arrangement, the circuit provides a signal path between a first and a second different layers of a multilayer. By providing one segment (26a) as a signal segment and another segment (26b) as a ground segment the size and shape of the electrically isolated segments (26a, 26b) can be selected to provide the interconnection circuit having a predetermined impedance characteristic. The interconnection circuit can thus be impedance matched to circuit board circuits, devices and transmission lines,

such as striplines, microstrips and co-planar waveguides. This results in an interconnection circuit which maintains the integrity of relatively high-frequency signals propagating through the interconnection circuit from the first layer to the second layer. The interconnect circuits can be formed by creating distinct conductor paths (26a, 26b) within the cylindrical plated through-holes (26) using variety of manufacturing techniques including, but not limited to, broaching techniques, electrostatic discharge milling (EDM) techniques and laser etching techniques.

WO 00/78105 A1



IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Published:

— *With international search report.*

MULTI-CONNECTION VIA

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GOVERNMENT RIGHTS

Not applicable.

RELATED APPLICATIONS

10 This application claims priority under 35 U.S.C. §119(e) from Application Nos. 60/138,730 and 60/139,063 each filed June 11, 1999 and Application No. _____ filed July 12, 1999 entitled Multi-Connection Via and Related Circuits and Techniques having named inventor Sepehr Kiani all of which are hereby incorporated herein by reference in their entirety.

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FIELD OF THE INVENTION

 This invention relates generally to electrical connections between layers of multi-layer printed circuit boards and more particularly to a class of layer-to-layer interconnections referred to as via circuits or more simply vias.

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BACKGROUND OF THE INVENTION

 As is known in the art, there exists a class of electrical connection structures, referred to as plated through holes (PTHs) or via circuits or more simply vias, which provide layer-to-layer interconnections in multi-layer printed circuit boards (PCBs).

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 A conventional via in a multi-layer PCB is typically provided by drilling or otherwise forming a hole through the PCB. The through hole passes through all conductive layer traces in the PCB which are intended to be connected. The hole is then plated to form an electrical connection among the conductive traces. In this
30 manner, electrical connections between layers of multi-layer PCBs can be provided.

This process can be used to provide a signal path through which a single signal propagates between layers of a PCB. Connections to conductive traces or signal paths in each of the PCB layers can be made. This via connection technique conserves space on the PCB and thus allows PCBs to be more densely populated.

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The via has been the mainstay of layer-to-layer interconnection since the inception of double-sided and multi-layer boards. Originally vias served dual purposes, providing layer-to-layer interconnect and through-hole component mount. The growth of surface mount component technology (with the exception of backplane connectors and other large devices), however, has reduced the need to utilize vias for through-hole component mount and has resulted in the via primarily providing layer-to-layer interconnection.

There has, however, been a trend to provide PCBs having increasingly higher circuit density and higher circuit speed. To help meet the demand for increased circuit density, it has been proposed to provide more than one independent signal path or connection in a single via. To provide multiple connections in the same via of a PCB, the via is formed as described above. Discrete connections are then formed among the conductive traces of the PCB by establishing grooves in the plating of the via to electrically isolate segments of the PCB. This technique permits two or more independent connections to be made in the same via of a multi-layer PCB. This technique further conserves space on the PCB and thus allows PCBs to be even more densely populated

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Despite the advances made in increasing circuit density on PCBs, the high performance requirements of modern integrated circuit (IC) devices impose requirements for increasingly higher density of interconnections on PCBs so that the PCBs can accept the large number of input and output signal lines from IC devices which are packaged into increasingly smaller volumes. All of these design and

performance considerations add to the difficulties in attempting to lower PCB production costs which are increasing due to the use of complicated multiple-layer substrates.

5 Furthermore, modern IC devices operates at increasingly higher frequencies. As clock frequencies of circuits used on PCBs exceed 100 MHz, the electrical characteristics of PCB traces resemble high-speed signal transmission lines rather than D.C. electrical circuits. The higher clock frequencies and resultant shorter signal rise times expose PCB performance limitations which are manifested by signal integrity
10 phenomena such as ringing, reflections, ground bounce, and crosstalk.

 State of the art computer motherboards operate at frequencies of 100MHz and above, while telecommunications and high performance systems use device to board frequencies an order of magnitude higher. High performance systems having chip-to-
15 board clock speeds in the GHz range are expected. To support these current and future performance demands, improvement gains in PCB technology are required.

 To address the above density and speed concerns "buildup technologies" such as photo-via redistribution, and sheet buildup, have been developed. These techniques
20 have increased PCB performance significantly. These techniques, however, rely on thinner layers and use chemical etching (photo-defined vias), laser ablation, or plasma etching technologies to drill holes and connect PC board layers. Thus, such techniques are not appropriate for use in PCBs which include a relatively large number of layers between signal paths which must be connected.

25 So-called micro-vias have also been proposed. Both the signal and density performance of micro-vias are very good in comparison to drilled vias. There are still discontinuities in the signal path, because the ground plane is disrupted. However, because the scale is so small, this problem is minimal, especially when only going

through one layer (which does not break the continuous ground path). Micro-vias are particularly useful in applications in which the number of PCB layers is relatively small or where density is extreme, such as in micro ball grid array (μ BGA) escapement. As an added benefit, micro-vias can be placed directly in a surface
5 mount pad.

Because micro-vias must be manufactured from the outer surface (often out of non-woven aramid reinforced layers or unreinforced dielectric), the micro-vias can only be on the outer traces unless subsequent layers are built on top of the constructed
10 panel. Each layer adds significant processing cost. Via depth is limited greatly because the plating chemistry cannot flow through small blind holes in the same manner as through-hole vias. Similar limitations exist for laser ablated and co-deposition vias. Thus, micro-vias are also not particularly useful in PCBs which include a relatively large number of layers between signal paths which must be
15 connected.

Furthermore, none of the above techniques address the problem of maintaining signal strength and quality (i.e. shape of signal, lack of noise from either internal reflections or cross talk from other lines) collectively referred to herein as signal
20 integrity as device operating frequencies increase and/or clock rise times decrease. Moreover, owing to the addition of noise as well as reflections due to impedance mismatches, signal quality suffers when the impedance of the layer-to-layer interconnection transmission structure changes, resulting in parasitic wave reflections and in some cases resonance. This results in a signal path having a relatively high
25 insertion loss characteristic. A secondary related effect is crosstalk, which relates to the electro-magnetic interference (EMI) between circuit structures. Thus, one problem with the prior art approaches, is that they merely attempt to increase density on a printed circuit board and they fail to provide any mechanisms for maintaining signal integrity and signal quality.

It would, therefore, be desirable to provide an interconnection structure which provides a layer-to-layer signal path which is relatively low loss, which does not degrade signal performance, which maintains signal integrity and which allows increased density of connections. It would also be desirable to provide an interconnection structure which is easily adapted to work with existing PCB manufacturing techniques, components and the like.

It would further be desirable to provide an interconnection structure which reduces the number and magnitude of impedance discontinuities due to transmission structure changes and which reduces the amount of crosstalk between circuit structures.

SUMMARY OF THE INVENTION

It has, in accordance with the present invention, been recognized that although signal lines within a single printed circuit board (PCB) layer are provided having predetermined impedance characteristics (i.e. the impedance of the signal line is controlled), such impedance control is not available for conventional plated-through holes (PTHs) which are used to provide signal paths between different layers of the PCB. This lack of control of the impedance characteristics of the via results in relatively large impedance mismatches between the via and other circuits/circuitry. Thus, the vias have relatively high insertion loss characteristics due primarily to impedance mismatch.

Because the via are lossy, there has been a desire and need to minimize number of vias on PCBs. In an effort to minimize the number of vias, circuit traces are ideally limited to a single plane (i.e. a single layer) in the PCB. Limiting the

circuit traces to a single plane, however also limits the number of possible circuit layout which are available to a circuit board designer.

In accordance with the present invention, an interconnection structure for providing a signal path between a first layer and a second different layer of a multi-layer structure includes a via having a plurality of electrically isolated segments with at least one of the electrically isolated segments coupled to a signal path and at least one of the electrically isolated segments coupled to ground. With this particular arrangement, a multi-connection via (MCV) which does not degrade signal performance, signal integrity or signal quality of relatively high frequency signals is provided. By coupling a first segment of the via to a signal path and having a second segment of the via in proximity to the first segment coupled to ground, a defined electric field pattern is established in the via when signals having a relatively high frequency propagate through the via. By providing a structure through which a signal can propagate with a defined electric field pattern, the MCV provides a signal path having a relatively low insertion loss characteristic to relatively high frequency signals propagating therethrough. The impedance characteristic of the via can be selected by appropriately selecting a variety of via characteristics including but not limited to the hole diameter of the via and the relative widths of the signal and ground segments.

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This allows manufacture of printed circuit boards (PCBs) which include vias having a relatively low insertion loss characteristic and a relatively low return loss characteristic. The vias provide signal paths having a relatively low insertion loss characteristic because the vias can be designed and manufactured having defined impedance characteristics. The via can thus be designed to better match (in an impedance matching sense) the IC devices or circuits or signal paths coupled thereto. Because the via of the present invention provides a relatively low loss, reliable signal path between layers of a multi-layer printed circuit board, it is not necessary to restrict

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the PCB circuit layouts to a single layer or plane. Consequently reducing the number of required layers in a PCB.

Furthermore the MCV of the present invention can be provided having
5 multiple signal segments and/or multiple ground segments to thus allow inclusion of more signal traces in a single via. This allows the manufacture of PCBs having relatively high circuit density. The MCV of the present invention allows impedance control of signal paths between layers of a multi-layer PCB and thereby allows use of a connector which integrates tightly with the PCB. This type of impedance control is
10 not possible with conventional via technologies, including advanced structures such as micro vias. Thus the MCV of the present invention. This ability fundamentally changes routing rules for high speed signal traces, allowing for layer changes without concern of signal degradation. Furthermore, signal performance of the co-cylindrical wave-guide structure is completely independent of diameter. Moreover, MCVs
15 having multiple signal and ground segments which provide improved electrical performance allow further increases in connection density.

The MCV may be considered as a "shielded via" which offers improved performance to connectors and devices without requiring design changes of the PCB,
20 connectors or devices. That is, the MCV of the present invention is compatible with conventional PCB manufacturing processes including PCB via manufacturing processes.

To construct multi-connection vias in PCBs for signal experiments, a broach
25 process can be used to segment plated-through holes to provide isolated segments. Alternatively, MCVs can be provided using an electrical discharge machining (EDM) process. In utilizing the EDM process it should be noted that to properly utilize an EDM process to manufacture the multi-connection vias, it is necessary to provide a signal path from each of the individual segments of the via to ground during the EDM

process.

In accordance with a still further aspect of the present invention a method of routing signal traces in multi-layer printed circuit board using a multi-connection via (MCV) includes the steps of providing a multi-connection via having at least a pair of signal segments and at least one ground segment, connecting a first signal trace to a first one of the pair of signal segments, connecting a second signal trace to a second different one of the pair of signal segments and connecting the ground segment to a groundplane layer of the multi-layer printed circuit board. With this arrangement, a technique for reducing the number of vias provided in a multi-layer printed circuit board to route signal traces between different layers of the multi-layer printed circuit board is provided. This routing technique utilizing MCVs finds particular applicability when routing high speed signal traces in PCBs and maintaining signal integrity is an important concern.

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In accordance with a still further aspect of the present invention, a multi-connection via launch includes a connector having a signal contact and ground contact disposed in an MCV. The MCV includes a ground via segment coupled to a ground plane and the ground contact of the connector and a signal via segment coupled to a signal trace and the signal contact of the connector. Since the impedance characteristics of the MCV can be controlled, the MCV can act as an impedance matching structure between the connector and the signal trace on the PCB. This arrangement solves the problem of device and connector launch to the PCB which represents a major discontinuity in a signal path. The performance benefits provided by the MCV's impedance-controlled structure throughout the transition thus carry over to PCB connector and device launches.

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BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing features of the invention, as well as the invention itself may be more fully understood from the following detailed description of the drawings, in which:

5 FIG. 1 is a perspective diagrammatical view of a multi-connection via;

FIG. 1A is a perspective diagrammatical view of a multi-connection via;

FIG. 1B is a top view of a symmetrically split multi-connection via;

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FIG. 1C is a top view of a non-symmetrically split multi-connection via;

FIG. 1D is a diagrammatical perspective view of a multi-connection via launch;

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FIGs. 2 – 2C are a series of top views illustrating different single-ended via structures;

FIGs. 3 – 3E are a series of top views illustrating different examples of
20 differential via structures;

FIGs. 4-4B are a series of views illustrating clusters of multi-connection vias;

FIG. 5 is a diagrammatical illustration of a parallel split pads;

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FIG. 6 is a diagrammatical illustration of a radial split pads;

FIGs. 7A – 7C are a series of views illustrating a pad stack prior to drilling and plating steps;

FIGs. 8A – 8C are a series of views illustrating a pad stack after drilling and plating steps;

5 FIG. 9 is a perspective view of a two-dimensional split via;

FIGs. 10 and 10A are a series of diagrammatical perspective views of in via signal traces;

10 FIG. 11 is a perspective view of a buried multi-connection via;

FIGs. 12-12E are a series of plan views illustrating signal trace routing paths through vias;

15 FIG. 13 is a perspective view of a connector having a plurality of contact pairs press fit into a multi-connection via;

FIG. 13A is a cross-sectional view of a differential connection in a multi-connection via;

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FIG. 13B is a cross-sectional view of a single-ended connection in a multi-connection via;

FIG. 13C is a perspective view of a connector having a triplet contacts press fit
25 into a multi-connection via;

FIG. 13D is a cross-sectional view of a differential connection in a multi-connection via;

FIG. 14 is a perspective view of a connector having a pair of signal contacts and a pair of ground contacts press fit into a multi-connection via;

FIG. 14A is a cross-sectional view of the connector of FIG. 14 after insertion
5 into the multi-connection via;

FIG. 15 is a perspective view of a connector having an eye of the needle connector disposed above a multi-connection via;

FIG. 15A is a cross-sectional view of the connector of FIG. 15 after insertion
10 into the multi-connection via;

FIG. 16 is a cross-sectional view of a single-ended co-cylindrical waveguide;

FIG. 17 is a cross-sectional view of a differential co-cylindrical
15 waveguide;

FIGs. 18 and 18A are a series of perspective views which show a surface
mount device disposed over and on, respectively, a multi-connection via;
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FIGs. 19 and 19A are a series of perspective views which show a surface
mount device having an eye of the needle connector disposed over and on,
respectively, a multi-connection via;

FIG. 20 is a perspective view of a surface mount capacitor disposed over a
25 multi-connection via;

FIG. 21 is a perspective view of surface mount connector coupled to surface
mount pads of multi-connection vias provided in a multi-layer printed circuit board;

FIG. 21A is a top view of a multi-connection via provided in the second printed circuit board shown in FIG. 21;

5 FIG. 22 is a perspective view of a first printed circuit board having surface mount connectors coupled to multi-connection vias on a second printed circuit board;

FIG. 22A is a top view of a multi-connection via provided in the second printed circuit board shown in FIG. 21; and

10 FIG. 23 is a top view of a multi-connection via provided in a printed circuit board.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

15 Before proceeding with a description of the figures, it should be noted that reference is sometimes made herein to multi-connection vias (MCVs) manufactured in a printed circuit board or multi-layer structure made from a particular material such as FR4. Those of ordinary skill in the art should appreciate that other materials suitable for manufacture of printed circuit boards and multi-layer structures may also be used.

20 Reference is also sometimes made herein to MCVs having a particular cross sectional diameter. It should be understood that MCVs having any diameter may be used. Also, MCVs having a substantially round cross-sectional shape are herein described. It should be appreciated that MCVs having other shapes including but not limited to oval, rectangular, square, triangular and irregularly shapes may also be used.

25 Referring now to FIG. 1, a multi-layer printed circuit board (PCB) 10 (also sometimes referred to herein as a multi-layer structure 10) includes a plurality of layers 12a-12h, generally denoted 12 each of which corresponds to a ground plane layer. Each of the ground plane layers 12 may be provided from a conductive material

(e.g. a sheet of copper foil) which is typically supported by a support structure such as a dielectric core material, for example. The ground plane layers 12 may be disposed, deposited, attached or otherwise provided on the support structures using any well-known technique. PCB 10 also includes a plurality of signal traces 14a – 14c, generally denoted 14 which are disposed on different signal layers of the PCB 10. It should be noted that in FIG. 1, to promote clarity in the figure, the dielectric cores or other structures which support each of the ground plane layers 12 and the signal traces 14 are not shown. By way of terminology, the layers of PCB 10 on which signal traces (such as signal traces 14a – 14c) are disposed are referred to as signal trace layers or more simply signal layers. Similarly, the layers of PCB 10 on which are disposed ground planes (such as ground planes 12) are sometimes referred to as ground planes or more simply ground layers. Similarly again, the layers of PCB 10 on which power signals are disposed are sometimes referred to as power layers or power planes.

Although the signal traces 14a, 14c are disposed on different layers of the multi-layer structure 10, they are electrically coupled through an interconnection device 16. Interconnection device 16 is a multi-connection via (MCV) 16 which can provide multiple signal paths between any of the signal traces 14 on any signal layer of the multi-layer structure 10. MCV 16 is provided from conductive material disposed on the walls of an opening in the multi-layer structure. The conductive material is disposed to form a plurality of separate segments 18a, 18b, 20a, 20b which are electrically isolated from each other. Although MCV 16 is here shown having four electrically isolated segments 18a, 18b, 20a, 20b, it should be appreciated that MCV 16 can be provided having fewer or greater than four segments. The particular number of segments to be provided in an MCV depends upon a variety of factors including, but not limited to, the particular application, the number of signal traces to be connected and the limits on mechanical tolerances and printed circuit board processes imposed by manufacturing techniques.

In one embodiment, the opening in the multi-layered structure 10 is provided as a conventional plated through hole (PTH) which is then "split" to provide the electrically isolated segments. It should be noted that portions of the layers 12 and interconnection device 16 have here been removed to promote clarity in the figure. Thus, a portion of segment 20b is shown in phantom and in this particular embodiment, segment 20b has a size, shape and function similar to segment 20a. Segments 18a, 18b have pad regions 19 (or more simply pads 19) while segments 20a, 20b have pads 21a – 21d generally denoted 21. The purpose of the pads 19, 21 will be described below.

In this particular embodiment, segments 18a, 18b, 20a, 20b are electrically isolated from each other by providing spaces or splits generally denoted 22 between each of the segment 18a, 18b, 20a, 20b, in the MCV 16. In this example, split 22a is between segments 18b and 20a, split 22b is between segments 20a and 18a, split 22c (only partially visible in FIG. 1) is between segments 18a and 20b and split 22d (not visible in FIG. 1) is between segments 20b and 18b. It should be noted that a variety of different manufacturing techniques can be used to electrically isolate the segments 18a, 18b, 20a, 20b. Thus, the term "split" should not be misconstrued to imply that the only technique to provide the electrically isolated segments 18a, 18b, 20a, 20b is mechanical cutting or splitting of the conductive material which forms the walls of the hole in the multi-layer structure 10.

It should also be noted that a variety of different techniques for manufacturing the isolated segments 18a, 18b, 20a, 20b, including, but not limited to, abrasive waterjet cutting, broaching, laser machining, milling, EDM, ultrasonic machining, selective patterning or deposition, selective plating and chemical etching processes can be used. Also, so-called non plating processes involving the use of conductive inks applied by either printing or screening processes can also be used.

It should further be noted that the operation and advantages of the MCV 16 as well as other MCV structures described herein are independent of the particular manufacturing techniques used to provide the MCVs. Any manufacturing technique including but not limited to those mentioned above, which can reliably be used to manufacture high quality, reliable MCVs and PCBs may be used. The particular manufacturing technique which is used in any application will depend on a variety of factors including but not limited to the purpose of the particular application (e.g. space, military, commercial), the cost of the manufacturing process (including development costs as well as the costs of start-up tooling or machinery) compatibility with standard PCB manufacturing processes, the quality with which the MCVs and PCBs can be manufactured compared with the quality of the MCVs and PCBs required for the application, production rate required for a particular application, circuit geometry generation capabilities vs. circuit geometry required in any particular application and control and scale of feature parameters of the MCV and PCB.

Since the segments 18a, 18b, 20a, 20b are electrically isolated, the segments may be independently coupled to different circuit structures or components (e.g. signal or ground paths, IC devices, etc...) of the multilayer structure 10. As shown in FIG. 1, segments 18a, 18b are each coupled to ground plane 12a via pads 19. Thus, segments 18a, 18b are effectively coupled through the ground plane 12a on PCB 12a. Similarly, segments 20a, 20b are coupled to respective ones of the signal paths 14a, 14b through pads 21b, 21c.

Pad 21a is disposed on a top layer dielectric layer of PCB 10 and pad 21d is disposed on a bottom dielectric layer of the PCB 10. Pads 21a, 21d are not coupled to signal traces. It should be noted that in some applications it may be desirable to provide pads 21a, 21d having a size and shape which is different than the size and shape of pads 21b, 21c. As will be described further below in conjunction with FIG.

1C and FIGs. 7-8C, the widths W_s of pads 21a-21d are selected to both accommodate mechanical tolerances in the manufacture of MCVs and to help provide a good impedance match to the respective signal path or circuit component coupled thereto.

5 It should be appreciated that portions 24a, 24b of each of the ground plane layers 12 of PCB 10 are removed over the regions where the signal segments 20a, 20b of the MCV exist to help reduce impedance discontinuities and control impedance values in the signal segments 20a, 20b.

10 As mentioned above, signal paths 14a and 14c are on layers of different ones of the PCBs 12. Each of the signal traces 14a, 14c have a first end coupled to respective ones of pads 21b, 21c which in turn are coupled to signal segment 20a. Thus, signal segment 20a provides an electrically conductive signal path between signal traces 14a and 14c.

15 The impedance characteristics of segment 20a presented to signal paths 14a, 14b can be controlled by selection of the dimensions of the MCV structure 16. In particular, by selecting the relative shapes and dimensions of the signal segments and ground segments as well as the shapes and dimensions in the openings in the ground
20 plane layers (e.g. portions 24a, 24b) the MCV can be provided having signal path performance characteristics required for supporting the signal bandwidth of current and future devices used in multi-layer structures such as multi-layer structure 10. As is known, there is a trend to use devices which operate at increasingly high clock frequencies. As high frequency signals propagate along signal traces of PCBs, the
25 integrity of the signals as they traverse between different layers of a multi-layer structure must be preserved. The impedance-controlled MCV structures 16 of the present invention provide appropriate vehicles for such transmission.

If a signal path is perfectly impedance matched, the signal will experience no

impedance transitions which provide points of energy loss. The only losses in a perfectly impedance matched signal path are those from the dielectric (i.e. attenuation), which are length-of-trace dependent. Attenuation is a significant problem in relatively large PCBs, such as backplanes, where the trace lengths of the signal paths are long compared to the wavelength of the signal. When there are impedance discontinuities in the signal path, additional energy is lost and the signal propagating along the path is weakened. This lost energy has several effects on the circuit.

First, part of the signal is reflected back towards the source. This reflection can manifest itself as noise on the signal path. If two impedance mismatches are spaced by a distance approximately an integer multiple of a quarter-wavelength of the signal frequency, the reflections will resonate between the impedance mismatches. A common case is that of short unterminated lines (also sometimes referred to as stubs), where the signal propagates to the end of a signal trace that is terminated in either an open or a short circuit (i.e. the end of the signal trace is not connected to any structure intended to provide an impedance matching function) thereby causing all of the signal energy to be reflected.

Second, if the signal path is not fully controlled (e.g., completely bound by ground structures) within the range of other signal carrying lines, electromagnetic interference (EMI) will result. EMI reduces the energy of the signal, and these free energy waves cause or induce crosstalk to other circuits. Crosstalk refers to the inducement or coupling of a signal from one signal trace or line to another signal trace or line. A crosstalk signal is a signal which is induced on one signal line from the electromagnetic field surrounding a signal line on which a signal is propagating. A crosstalk signal can occur from between a board and a device above the board and manifest itself as noise on signal lines physically proximate to the signal line on which a signal was originally propagating. Devices typically have maximum noise levels

which they will safely tolerate before erratic behavior occurs and crosstalk can be a significant source of noise. Crosstalk can thus be a source of device and PCB malfunction. The impedance controlled MCV structures of the present invention can, therefore, help reduce this problem.

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Referring now to FIG. 1A a multi-layer structure 10' having a plurality of layers 12' has provided therein an MCV 26 which includes a signal segment 26a and a ground segment 26b coupled to pads 27. In FIG. 1A, a plurality of dielectric cores 28 which act as the support structures for ground plane layers 12' and signal traces 14' are shown. It should be noted that dielectric support structure 29 is disposed above the pad 28b and below the pad 28a (i.e. the pad 28a lies on a top surface 29a of the support structure 29 while a bottom surface of the support structure 29 lies on the top surface of the pad 28b). The MCV 26 can be formed using a drill, plate and split process to provide the segments 26a, 26b while subtractive (e.g. etching) or additive (e.g. deposition) techniques can be used to provide the pads 27. In this embodiment, PCB 10' includes at least two layers which correspond to signal layers of the multi-layer structure 25. The MCV 26 provides a signal path between a first signal trace 27a on one signal layer of the multi-layer structure 25 and a second signal trace 27b on a different signal layer of the multi-layer structure 25. The signal traces 27a, 27b are typically provided as conductive material deposited or otherwise provided on the signal layers of the multi-layer structure using conventional deposition or etching techniques. The signal traces 27a, 27b may be provided in any printed circuit transmission line configuration including but not limited to stripline, microstrip and co-planar waveguide configurations.

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Referring now to FIG. 1B in which like elements of the MCV 26 in FIG. 1A are provided having like reference designations, the MCV 26 has a diameter D, a plating thickness T_p and includes the signal and ground segments 26a, 26b and pads 28a, 28b.

As can be clearly seen in FIG. 1B, the MCV 26, has a non-symmetric geometry in which the arc length L_s of the signal segment 26a is smaller than the arc length L_g of the ground segment 26b. As can also be clearly seen in FIG. 1B, the ground plane layer 12' has a portion thereof removed to provide the region 24 in which is exposed a surface 25a of the dielectric support structure 28. Each of the ground plane layers 12' (FIG. 1A) are also provided having portions thereof removed to expose regions of the dielectric core or support structure proximate the MCV.

The reflection and transmission characteristics of the MCV 26 can be controlled by varying the width W_{gap} of the regions 29, and the arc lengths or widths L_s , L_g of the signal and ground segments 26a, 26b and the size and shape of the regions 24. It has been found that the MCVs are provided having favorable electrical characteristics of when the arc length of the signal segments are narrower than the arc length of the ground segments.

It should be appreciated that the multi-connection via structure can be considered as having a co-cylindrical waveguide structure which is analogous to the structure of a co-planar waveguide. As in a co-planar waveguide, a co-cylindrical waveguide maintains impedance control between signal and ground segments. Thus, in a manner similar to a co-planar waveguide, the multi-connection co-cylindrical waveguide via structures achieve impedance match by controlling diameter, signal arc length and gap relative to ground segment and ground plane clearances.

Referring now to FIG. 1C, an MCV 26' is shown having a symmetric geometry in which the MCV 26' is split symmetrically about a central horizontal axis 28 of the MCV 26' to provide a pair of nonconductive regions 29a, 29b (also referred to as spaces or gaps) which electrically isolate the signal segment 26a' and the ground segment 26b'. The signal segment 26a and ground segment 26b are thus provided

having equal arc lengths L_s , L_g respectively. Regions 29a, 29b may be provided as dielectric regions (e.g. provided from portions of a PCB in which the MCV 26' is formed) or from air filled spaces.

5 In one particular example, a symmetrically split MCV 26 was provided having a diameter of about 0.559 mm and the width of gap regions 29a, 29b was varied. When the gap increased, the signal conductor and ground conductor arc lengths were decreased by an equal amount to thus maintain symmetry. The closest coupling
10 W_{gap} of the gap 29a, 29b has a significant effect on such coupling and therefore on reflection and transmission characteristics of the MCV. The best results were achieved with a gap width of about 254 μm .

15 Examination of test results reveals that the reflections drop off to near zero as the gaps 29a, 29b were widened until a gap width was reached at which the reflection was a minimum. It is expected, however, that if the gaps were widened beyond a certain point, (requiring a larger diameter MCV) the reflected power would eventually increase.

20 The energy that is reflected in a conventional PTH increases at a greater rate than that of MCVs with frequency. Thus the benefits of the MCV structure is greater at higher frequencies. In a best-tuned case, the reflected energy by the MCV is negligible across the frequency range. The stubs formed by those portions of the multi-connection via segments which extend above and below the signal traces
25 coupled to the via segments can dominate reflection characteristics of the MCV. Relatively large reflections can occur at frequencies corresponding to resonant frequencies of the stubs. In some cases pads (e.g. pads 21a, 21d in FIG. 1) at the end of the MCV may also be a source of reflections..

Examination of experimental test results show that transmission is consistent with the reflections. A decrease in reflected power increases the transmitted power proportionally. This is an important interaction to note, since it is possible to decrease both the reflection and the transmission. e.g. if losses due to EMI are high.

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Examination of experimental results to determine the affect of varying the conductor ratio on reflections and transmissions shows that varying the arc length L_s of the signal conductor 26a tunes the MCV structure somewhat better than varying the width W_{gap} of the gaps 29a, 29b and keeping the arc lengths L_s , L_g of the ground and
10 signal segments 26a, 26b symmetric. In this case, as the signal arc-length decreases below 520 μm , the reflections begin to increase at higher frequencies. This implies that these via structures are inherently tunable to the circuit to which the MCV is coupled (e.g. transmission lines 27a, 27b in FIG. 1A). Conventional PTHs can attain some performance gains by decreasing the size and increasing the ground clearance,
15 (both of which are difficult to achieve) but otherwise provide no means for true impedance tuning.

Examination of experimental test results to determine the affects of varying the diameter of MCVs on reflections and transmissions reveals that reducing the signal
20 arc length L_s reduces reflections to the same range as MCVs having smaller diameters. Thus, an MCV having a relatively large cross-sectional diameter is as tunable as an MCV having a relatively small cross-sectional diameter. This is in contrast to conventional PTH approaches in which increasing the via diameter increases the reflections and decreases the transmission, thus indicating sensitivity to diameter.

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The above tuning characteristic of MCVs is significant in that it indicates that larger diameter MCVs, which are easier to manufacture, employ better impedance control than the smallest conventional PTH. In other words, reflections and transmission in conventional PTHs are highly sensitive to cross-sectional diameter,
30 while impedance-tuned MCVs are not.

Referring now to FIG. 1D, a connector 30 having a signal contact 32 and ground contact 34 partially disposed in an MCV 36 provides a multi-connection via launch (an MCV launch). The MCV 36 is provided in a portion of a printed circuit board (PCB) 37 which may be provided from a dielectric material such as FR4 or any other material having similar mechanical and electrical characteristics or otherwise suitable for manufacture of PCBs. The MCV 36 includes a ground via segment 38 coupled to a ground plane 39 and a signal via segment 40 having a signal trace 42 coupled thereto.

In one particular example, the MCV launch is provided having a diameter of about 1.5 mm since at this diameter the MCV launch is easily manufactured and provides space for a pair of contacts. The arc length of the signal via segment 40 is selected to be about 540 μm and the gap or split 43 between the ground via segment 38 and the signal via segment 40 is about 254 μm . A signal is launched into the PCB signal trace 42 and exits on a connector (the launch portion of which is shown in FIG. 1D) both of which are impedance matched to 50 Ω . With these parameters, a relatively good impedance match is provided between the connector and the PCB signal trace 42.

Since the impedance characteristics of the MCV 36 can be controlled, the MCV 36 can act as an impedance matching structure between the connector and the signal trace 42 on the PCB. This arrangement solves the problem of device and connector launch to the PCB which represents a major discontinuity in a signal path. The performance benefits provided by the MCV's impedance-controlled structure throughout the transition thus carry over to PCB connector and device launches.

Referring now to FIGs. 2 – 2C a series of views illustrating single end via structures are shown. In FIGs. 2-2C, like reference designations correspond to like

elements throughout the several views. As shown in FIG. 2, an MCV 44 includes a signal line segment 45 and a ground segment 46 which are electrically isolated from each other. It should be noted that in this particular embodiment, the signal and ground segments 45, 46 are provided having equal arc lengths (also sometimes referred to herein as "widths"). The signal and ground segments 45, 46 are provided by forming a hole in a PCB and depositing, plating or otherwise providing conductive material on the surface of the PCB which defines the hole. The signal and ground segments 45, 46 are electrically isolated by forming non-conductive regions 48. Regions 48 represent printed circuit board areas exposed during drilling and/or other procedures performed to provide the MCV 44 and the nonconductive spaces 52 between the signal line segments 45 and the ground segment 46. To prevent exposed PCB regions 48 (and in particular surface 52) from absorbing moisture and to otherwise protect the regions 48 (and in some cases to strengthen the MCV 44), a central region 50 of the MCV 44 is filled with a material which may, for example be provided as a dielectric material such as an epoxy. It should be noted that in some applications, sealing may not be required..

A ground plane 53 is disposed about MCV 44 and electrically contacts the ground segment 46. Regions of the ground plane 53 have been removed to provide nonconductive areas 54. As explained above in conjunction with FIG. 1, in preferred embodiments, no conductive material is present in the region of a signal line 56 contacting the signal line segment 45 and thus the ground plane 53 is provided having a non-symmetric pattern in the region of the MCV.

The width of the gaps 52, the arc lengths of the signal and ground segments 45, 46, the diameter of the hole 48 and the layer combinations (e.g. thickness, relative dielectric constant, number of layers, etc...) of the PCB may all be varied to provide the MCV 44 having a predetermined impedance characteristic.

Referring now to FIG. 2A, it should be noted that the signal and ground segments 45, 46 are provided having un-equal arc lengths. In this particular embodiment, the arc length of signal segment 45 is smaller than the arc length of ground segment 46. In other embodiments, however, it may be desirable to provide signal segment 45 with an arc length which is greater than the arc length of ground segment 46. In this case, other features (e.g. spacing between the ground and signal segments, 45, 46, diameter of the MCV, etc. can be selected to provide an MCV having an appropriate impedance characteristic.

The MCV embodiments of FIGs. 2 and 2A were tested by providing layer connections between like spaced layers signal layers. The signal arc length was varied but the diameters of the MCVs were kept the same in all tests.

The results of the tests are summarized in Table I below which shows the reflection amplitude for a variety of different signal conductor arc lengths for MCVs having a diameter of 1.5mm.

Table I

Signal conductor arc length	Reflection amplitude
0.19mm	2.0%
0.31mm	1.0%
0.49mm	2.2%
0.74mm	3.6%
0.90mm	3.0%
1.09mm	8.4%
2.13mm	12.7%

Examination of Table I reveals that an MCV having a relatively large diameter with a wide signal conductor arc length has worse performance than a via having a smaller diameter. As the arc length is decreased, the reflection reduces to near zero

(in the case where L_s equals 0.31mm) and then the reflection increases again (in the case where L_s equals 0.19mm). It is interesting to note that in digital electronics, vias are capacitive in nature (i.e., yielded negative broadband reflection), while the over compensated multi-connection via here is inductive.

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Referring now to FIG. 2B, an MCV 44 includes a pair of signal segments 45 and a pair of ground segments 46 symmetrically disposed about a central longitudinal axis 49 of the MCV 44. The signal and ground segments 45, 46 are each provided having equal arc lengths. It should be noted however, that in some applications it may not be desirable or necessary to provide the signal and ground segments having equal arc lengths. For example, the width of the signal segment may be selected to correspond to the width of a signal trace which terminates on the signal segment of the MCV.

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Referring now to FIG. 2C, an MCV 44 includes triplet signal segments 45 and triplet ground segments 46 symmetrically disposed about a central longitudinal axis 49 of the MCV 44. The signal and ground segments 45, 46 are each provided having equal arc lengths.

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Referring now to FIGs. 3 – 3E a series of views illustrating differential via structures are shown. The primary difference between a single-ended MCV and a differential MCV is that in a single-ended MCV the signal propagates between ground return structures. In the differential case, the return path is a discrete conductor equal and opposite to another conductor. The ground in a differential signal acts as a drain for leakage caused by symmetry imperfections. In PCBs which include circuit components operating at relatively high clock speed (i.e. high-frequency circuits) differential signal pairing may provide performance advantages, especially for long traces. In FIGs. 3-3E, like reference designations correspond to like elements throughout the several views.

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As shown in FIG. 3, an MCV 60 includes signal line segments 61a, 61b which are provided by plating, depositing or otherwise adhering a conductive material to the walls of a hole formed in a PCB. The central portion 62 of MCV 60 is filled with a dielectric such as air or an epoxy. Portions 63 represent printed circuit board areas exposed during drilling and other procedures to provide the MCV 60 and the signal line segments 61a, 61b. It should be noted that in this particular embodiment, the signal line segments 61a, 61b are provided having equal arc lengths. In the case where the structure is for a differential signal the signal segments must be symmetric to achieve desired transmission and reflection characteristics.

A ground plane 64 is disposed about MCV 60. Although not shown in this view, it will be appreciated by one of ordinary skill in the art that multiple layers of the PCB in which the MCV exists may correspond to ground plane layers. This is also true of each of the embodiments of FIGs. 3-3E. Signal lines 58a, 58b and signal line segments 61a, 61b to which the signal lines 58a, 58b are respectively coupled are on different layers than the ground plane 64 and thus are electrically isolated from the ground plane 64. In FIG. 3, one differential signal pair (i.e. signal lines 58a, 58b) couples to MCV 60 on one signal layer and a second differential signal pair (not visible in FIG. 3) couples to MCV 60 on a second different signal layer. Portions of the ground plane 64 have been removed to provide nonconductive areas 65. It should be noted that signal lines 58a, 58b connect to MCV segments 61a, 61b toward a first end of the segments 61a, 61b. It should be noted that the traces coming into a differential via will also be of differential construction (e.g. differential stripline or microstrip construction). Thus, the signal traces will have a particular spacing which ideally will be maintained right up to the via.

The width of the gaps 63, the arc lengths of the signal segments 61a, 61b, the diameter of the hole 62, ground clearance distance and shape 65, and the layer

combinations (e.g. thickness, relative dielectric constant, number of layers, etc...) of the PCB may all be selected to provide MCV 60 having a predetermined impedance characteristic.

5 Referring now to FIG. 3A, it should be noted that in this embodiment, a ground segment 64a is disposed between two ends of the differential signal paths 61a, 61b. The signal and ground segments 61a, 61b and 64a are each provided having equal arc lengths.

10 The width of the gaps 63, the arc lengths of the signal segments 61a, 61b, and ground segments 64a, the diameter of the hole 62, ground clearance distance and shape 65, and the layer combinations (e.g. thickness, relative dielectric constant, number of layers, etc...) of the PCB may all be varied to impact the impedance characteristics of the MCV 60.

15 Referring now to FIG. 3B, it should be noted that in this embodiment, the ground segment 64a is disposed between two ends of the differential signal segments 61a, 61b. The signal segments 61a, 61b are each provided having equal arc lengths while the arc length of the ground segment 64a is smaller than the arc lengths of the
20 signal segments 61a, 61b. It should be noted that an equally effective alternative would be to provide the arc length of the ground segment 64a larger than the arc length of the signal segment.

As mentioned above in conjunction with FIG. 3A, the width of the gaps 63, the
25 arc lengths of the signal segments 61a, 61b, and ground segments 64a, the diameter of the hole 62, ground clearance distance and shape 65, and the layer combinations (e.g. thickness, relative dielectric constant, number of layers, etc...) of the PCB may all be varied to impact the impedance characteristics of the MCV 60.

Referring now to FIG. 3C, an MCV 60 includes signal line segments 61a – 61c which are provided in any suitable manner. In this particular embodiment, the signal line segments 61a – 61c are symmetrically disposed about a central longitudinal axis and are provided having equal arc lengths.

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The ground plane 64 is disposed about MCV 60 the signal lines 58a, 58b and signal line segments 61a – 61c to which the signal lines 58a – 58c are respectively coupled are on different layers than the ground plane 64 and thus are electrically isolated from the ground plane 64. Portions of the ground plane 64 have been removed to provide nonconductive areas 65. It should be noted that no drain is provided in this embodiment and that without a drain between multiple-differential pair sets, there is crosstalk. Thus, this embodiment would not be preferred.

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Referring now to FIG. 3D, an MCV 60 includes signal line segments 61a – 61f which are provided in any suitable manner. In this particular embodiment, the signal line segments 61a – 61f are symmetrically disposed about a central longitudinal axis and are provided having equal arc lengths. It should be noted that orientation of the signal line segments in each of FIGs. 3D and 3E can vary from hole to hole to provide the best trace routing in the PCB.

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The ground plane 64 is disposed about MCV 60 the signal lines 58a – 58f and signal line segments 61a – 61f to which the signal lines 58a – 58f are respectively coupled are on different layers than the ground plane 64 and thus are electrically isolated from the ground plane 64. Portions of the ground plane 64 have been removed to provide nonconductive areas 65. It should be noted that no drain is provided in this embodiment and that without a drain between multiple-differential pair sets, there is crosstalk. Thus, this embodiment would not be preferred.

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Referring now to FIG. 3E, an MCV 44 includes MCV signal line segments 61a – 61d a first ground segment 64a disposed between two the differential signal paths 61a, 61d and a second ground segment 64b disposed between two the differential signal paths 61b, 61c. The signal segments 61a – 61c are each provided having equal
5 first arc lengths and the ground segments 64a, 64b are each provided having equal second arc lengths. In some applications it may be desirable to make the first and second arc lengths equal lengths while in other embodiments it may be desirable to make the first and second arc lengths unequal(that is the differential pair signal segments should have equal arc lengths, but the ground drain can be provided having
10 and arc length which is either larger or smaller than the arc length of the signal segments.

In this particular embodiment, the ground segments 64a, 64b are diametrically opposed and the MCV signal line segments 61a – 61d are symmetrically disposed on
15 opposite sides of a plane of the MCV 60 which passes through ground segments 64a, 64b along a horizontal center line of the MCV 60.

The ground plane 64 is disposed about MCV 60 and the signal lines 58a – 58d and signal line segments 61a – 61d to which the signal lines 58a – 58d are respectively
20 coupled are on different layers than the ground plane 64 and thus are electrically isolated from the ground plane 64. Portions of the ground plane 64 have been removed to provide nonconductive areas 65. Ground segments 64a, 64b are coupled to ground plane 64. Because there is a ground drain between signal pairs experiments have show that there is no cross talk, therefore this configuration would be preferred
25 for multiple signal sets in a single via.

Referring now to FIGs. 4-4B in which like elements are provided having like reference designations throughout the several views, a series of clusters of multi-connection vias 66 are shown.

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Referring first to FIG. 4, a plurality of two-connection vias 66 clustered in pairs 67a, 67b define routing channels 68a, 68b which pass on either side of the clusters 67a, 67b. Ground vias 66a are juxtaposed with zero trace spacing between them. Because there is no need for a keep-out zone between the ground sides of the vias 66a, connection density increases.

Referring now to FIG. 4A, one electrical form of MCV that particularly benefits from multi-connection vias is the differential pair. In its simplest form, a differential pair MCV provides two connections over which can be transmitted signals in opposed phase. Because a perfectly balanced differential pair is not possible, it is desirable to have a ground drain close to the pair. FIG. 4A illustrates clusters 69a – 69d of three three-connection vias 60. Each three-connection includes a ground drain 70a and a differential pair (i.e. signal segments) 70b. The ground sides 70a of the MCVs 70 vias are juxtaposed in a zero trace condition and thus no keep-out zone is necessary thereby increasing connection density. The clusters 69a-69d are arranged to define routing channels 72a-72d which pass on either side of the clusters 69a-69d.

Referring now to FIG. 4B, a plurality of four-connection vias 76 are grouped in clusters 78a, 78b. Each four-connection via 76 includes a pair of ground drains 76a and a pair of signal segments 76b. The ground sides 76a of the MCVs 76 are juxtaposed in a repeating pattern which thus provides higher connection densities than prior art techniques. The clusters 78a, 78b are arranged to define a routing channel 80 which passes between the clusters 78a, 78b.

As demonstrated by the examples shown in FIGs. 4-4B, the possibilities for multi-connection via arrangements are numerous. One consideration in routing multi-connection vias is clearance around the via structure. The distance between the signal side (e.g. segments 76b) and the trace is much larger than that of the ground side (e.g. segments 76a), primarily due to the ground plane clearance. This clearance requires traces on the layers above and below the ground plane to not be routed in the

clearance areas, thereby avoiding potential impedance mismatch in the trace and minimizing crosstalk from the signal via. On the via ground side, the ground plane is uninterrupted, because there is little or no field on this side. Therefore, clearance on the ground side can be set to just outside a minimum annular ring requirement.

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It should be noted that the MCVs 66, 70 and 72 described above in conjunction with FIGs. 4-4B, may be provided having any of the appropriate geometries described above in conjunction with FIGs. 2 – 3E.

10 Referring now to FIG. 5, a multi-connector via 82 includes pad segments 82a-82f. The pad segments are each spaced by a gap 84. The gap edges 86 are parallel and thus provide so-called “parallel splits” between the pad segments 82a-82f.

The parallel split approach is in contrast to the so-called radial split approach as illustrated in FIG. 6. In the radial split approach, a multi-connector via 88 includes 15 pad segments 88a-88f. The pad segments 88a-88f are each spaced by a gap 84. The gap edges 89 are formed at an angle with respect to each other so that a straight line (here shown in phantom as lines 91) drawn along a plane defined by each edge 89 intersects a center point 90 which is located along a central longitudinal axis of the 20 MCV 88.

While MCVs with parallel and radial pad segments can be produced with equal ease, the parallel split provides greater arc length for traces to connect to. In some applications such additional arc length may be desirable since it may offer 25 additional flexibility, considering the difficulty in routing from a specific direction to the MCV.

Referring now to FIGs. 7 – 7C a series of views illustrating a pad stack prior to drilling and plating for a single conductor shielded via, where signal layers without connections have no pad.

5 Referring first to FIG. 7, a pattern to be etched or otherwise formed in top and bottom pad layers of a multilayer structure includes conductor regions 92 and 94 which will eventually correspond to a signal segment and a ground segment, respectively, of an MCV. Shown in phantom and indicated by reference numeral 95 is the diameter of hole to be drilled or otherwise provided (e.g. punched or cut) in a PCB
10 which will be plated to form the MVC.

As shown in FIG. 7A, a conductor region 96 having a radial shape is disposed on each layer of the multilayer structure which will include a signal trace to be coupled to the MVC. As shown in FIG. 7B, each layer of the multilayer structure
15 which will not include a signal trace does not include any conductor region in the area of the MVC. As shown in FIG. 7C a conductor region 97 provides a ground plane on the ground layers of the multilayer structure. Here portions 98 of the ground plane conductor 97 have been removed.

20 Once drilled, plated, and split, the pad stack appears as illustrated in FIGs. 8-8C. Referring first to FIG. 8, a hole 99 has been drilled through each of the layers. A portion of the conductor region 92 (FIG. 7) has been removed by the drilling process and the MCV signal segment 92' remains in the top and bottom pad layers as shown. Similarly, a portion of the conductor region 94 (FIG. 7) has been removed by the
25 drilling process and MCV ground segment 94' remains in the top and bottom pad layers. The plated through hole has been split to provide gaps 91 which define the signal and ground segments 92', 94'. As can be seen from FIGs. 8-8C, the splits 91 extend through each of the layers in the MVC.

As shown in FIG. 8A, a portion of the conductor region 96 (FIG. 7A) has been removed by the drilling process and an MCV signal segment 96' remains on each of the signal trace layers included in the multilayer structure. The signal segments 96' are each adapted to couple the MCV to a signal trace. As shown in FIG. 8B, each layer of the multilayer structure which will not include a signal trace still does not include any conductor region in the area of the MCV but does include a layer of conductive plating 93 disposed on the surface of the hole or "barrel" portion of the MCV. The plating material 93 is the conductor which electrically couples each of the layers through which the MCV passes. As shown in FIG. 8C the conductor region 97 provides a ground plane on the ground layers of the multilayer structure. The nonconductive region 98' is arranged above the signal segment pads 96' used to connect signal traces to the MCV.

Referring now to FIG. 9, a two-dimensional split via 100 including a multi-connection via 102 and a multi-connection via 104 are disposed within a multi-layer printed circuit board 110 as shown. The multi-connection via 102 includes a plurality of separate electrically isolated segments 106, each of which are connected to either a ground plane (not shown) or a signal trace (not shown) as required by the requisite circuitry of the printed circuit board 110 to connect circuitry (not shown) on one layer to another layer. The multi-connection via 104 includes a plurality of separate electrically isolated segments 108, each of which are connected to either a ground plane (not shown) or a signal trace (not shown) as required by the requisite circuitry of the printed circuit board 110 to connect circuitry (not shown) on one layer to another layer. The multi-connection via 102 and the multi-connection via 104 are disposed in the same hole within the printed circuit board 110, but electrically isolated from one another. A horizontal or radial split 105 exists between the two structures. In addition to increased layer-to-layer routing, horizontally-split vias can significantly reduce reflections caused by unused via extensions. In horizontal-split vias, each level operates as a separate set of connections, thereby improving space usage.

Referring now to FIGs. 10 and 10A, an alternative to splitting vias, is to create traces on the inside of a via cylindrical surface. It should be noted that in FIGs. 10 and 10A to promote clarity only conductive traces and segments are shown.

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As shown in FIG. 10, a signal trace 120 of one layer of a multi-layer printed circuit board can extend into a via 112 including a ground portion 116 and a signal portion 118 separated by a nonconductor 114 and connect to the signal portion 118. The signal portion 118 is also connected to a signal trace 122 on another layer of the multi-layer printed circuit board. With such an arrangement, a signal path from one layer can be connected to a signal path of another Layer and this arrangement also eliminates electrical stubs and EMI above and below the board from the via.

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As shown in FIG. 10A, a signal trace 120' of one layer of a multi-layer printed circuit board can extend into a via 112' including a ground portion 116 and a signal portion 118' and connect to the signal portion 118'. The signal traces 120', 122' approach MCV 112 from different angles on different layers of a multi-layer printed circuit board. The signal portion 118' of MCV 112 traverses in both horizontal and vertical directions (i.e. signal portion 120 "twists") to connect to a signal trace 120' to a signal trace 122'. With such an arrangement, a signal path from one PCB layer can be connected to a signal path extending at a different angle on another PCB layer. This technique can be used to provide flexibility in routing signal traces. For example, a signal trace must connect to a particular signal segment of an MCV and thus must be oriented in a particular manner relative the MCV. If the twist technique is used, then more options are available with respect to the orientation and location of MCV signal segments relative signal traces. The twist technique thus allows routing of signal traces to MCVs in the same manner that a signal trace would be routed to any plated through hole (i.e. without regard for the particular direction from which the signal trace intersects the via..

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Referring now to FIG. 11, a portion of a multi-connection via 124 embedded between layers of a multi-layer printed circuit board is shown. Such an embodiment is sometimes referred to as a "buried via." Although the buried via 124 is here shown providing connections between layer 125a, 125b, it should be appreciated that the via 124 could span more than two layers. The multi-connection via 124 includes a plurality of separate electrically isolated segments 126, each of which are connected to either a ground plane (not shown) or a signal trace (not shown) as required by the requisite circuitry of the printed circuit board to connect circuitry (not shown) on one layer to another layer.

With the use of the embedded multi-connection via 124, fewer vias are needed within the structure of the multi-layer printed circuit board to provide the same number of connections as can be made with conventional plated through holes. Thus the buried multi-connection via approach increases the connection density of the multi-layer printed circuit board. Furthermore, the buried multi-connection via approach eliminates electrical stubs from unused portions of vias thereby reducing or in some cases eliminating EMI above and below the board, and resin or some other appropriate sealant can be disposed in the via (by natural flow or by injection techniques) to seal exposed fiber edges in the split. Although not explicitly shown in FIG. 11, it should be appreciated that each of the segments 126 may have pads (such as pad 28a, 28b in FIG. 1A) coupled thereto to provide a means for contacting portions of ground or signal layers in the PCB.

Referring now to FIGS. 12 – 12E, signal routing techniques taking advantage of the inventive MCV are described. FIG. 12 shows known routing techniques with conventional PTHs or vias 130 to pass a signal from one layer of a printed circuit board (also referred to as a printed wiring it board) to another layer. Using conventional PTHs 130, first signal paths 132a enter the PTH 130 from a first

direction and second signal paths 132b enter the PTH 130 from a second direction which is orthogonal to the first direction. It should be noted that in each of FIGs. 12-12E, the traces enter the via on one layer and exit on another. It should also be noted that not all signal traces such as traces 132a are on the same layer nor are all signal traces such as signal traces 132b on the same layer.

FIG. 12A shows a routing technique using four MCVs 134 to route signal paths 132a from one layer of the printed circuit board to another layer. In this embodiment, each of the MCVs 134 include a ground segment 136 which can be connected to a ground plane layer on the printed circuit board and a signal segment 138 appropriately connected to signal paths 132a and 132b to route signals from the signal paths 132a and 132b. The signal paths 132a, 132b may each be on different layers of a multi-layer printed circuit board.

As shown in FIG 12B, the signal paths 132a, 132b can be routed using two MCVs 142a, 142b. Each of the MCVs includes a first and second signal segments 144, 148 and first and second ground segment 146, 150. Each of the ground segments 146, 150 is connected to the ground plane layer to provide a ground. The first signal segment 144 of MCV 142a is coupled to a pair of signal traces 132a, 132b to provide a first signal path through the first MCV 142a and the second signal segment 148 is connected to a pair of signal traces 132a, 132b to provide a second signal path through the MCV 142a.

Similarly, the first signal segment 144 of MCV 142b is coupled to a pair of signal traces 132a, 132b to provide a first signal path through the first MCV 142b and the second signal segment 148 is connected to a pair of signal traces 132a, 132b to provide a second signal path through the MCV 142b. It should be appreciated with such an arrangement, less vias need to be fabricated in the printed circuit board to provide a similar amount of signal paths, thus simplifying certain aspects of the

manufacturing requirements and processes, and increasing the space for routing the layers.

Referring to FIG. 12C, a prior art PTH 130' is used to route a pair of signal path 152a entering the PTH 130' from a first direction and a second pair of signal paths 152b entering the PTH 130 from a second direction which is aligned with the first direction.

FIG. 12D shows a routing technique using two MCVs 134' to route signal paths 152a from one layer of the printed circuit board to another layer. In this embodiment, each of the MCVs 134' include a ground segment 136' which can be connected to a ground plane layer on the printed circuit board and a signal segment 138' appropriately connected to signal paths 152a and 152b to route signals from the signal paths 152a and 152b. The signal paths 152a, 152b may each be on different layers of a multi-layer printed circuit board.

As shown in FIG 12E, the signal paths 152a, 152b can be routed using a single MCVs 142'. The MCV 142' includes first and second signal segments 144', 148' and first and second ground segment 146', 150'. Each of the ground segments 146', 150' are connected to a ground plane layer to provide a ground. The first signal segment 144' of MCV 142' is coupled to a pair of signal traces 152a, 152b to provide a first signal path through the MCV 142' and the second signal segment 148' is connected to a pair of signal traces 152a, 152b to provide a second signal path through the MCV 142'.

It should be appreciated with such an arrangement, fewer vias are required in the multilayer printed circuit board. Thus, the MCV reduces the number of vias required in a printed circuit board providing the same functionality of multiple PTHs and also while conserving valuable area on the printed circuit board, simplifying

certain aspects of the manufacturing requirements (e.g. since fewer plated through holes are required) and processes and allowing increases in connection density of the printed circuit board. It should, however, be noted that splitting the via is an added step which may result in somewhat increased complexity in the manufacture of the

5 PCB. In addition high speed performance characteristics are not attainable with conventional vias.

Referring now to FIGs. 13, 13A and 13B, having described various embodiments of a via with multiple conductors, it should now be appreciated, an

10 improved multi-connection connector 160 including a first contact 162 and a second contact 164 can be provided to mate with a plated through hole or via 168 disposed within a printed circuit board 166, the via 168 having a first separate electrically segment 172 which mates with contact 162 and a second separate electrically isolated segment 174 which mates with contact 164. As shown in FIG. 13A, the via 168 can

15 be arranged in a differential pair to provide two signal paths with segment 172 providing the first signal path and segment 174 providing the second signal path. Alternatively, as shown in FIG. 13B, the via 168 can be arranged with a signal segment 172' and a ground segment 174' to provide a single signal path. In this embodiment, contacts 162 and 164 press fit into the via 168 to provide connectivity

20 between the connector 160 and the printed circuit board 166 as shown.

For differential connections, it is desirable to have a ground structure close to the differential pair. Usually referred to as a drain, this ground structure provides return to stray signals due to imperfections in the differential pair. FIGs. 13C and 13D

25 shows an embodiment with connector elements that provide three connections required for a good differential pair. A pressfit connector 176 includes a first signal contact 178, a second signal contact 182 and a ground contact 180 that will mate with a plated through hole or via 186 disposed within a printed circuit board 184. The via 186 includes a first signal segment 188 which mates with contact 178, a second signal

segment 200 which mates with contact 182 and a ground segment 190 which mates with ground contact 180. The latter arrangement provides a ground path is close proximity to the signal path. A pressfit connection is shown but a soldered-in connector could also be used.

5

Referring now to FIGs. 14 and 14A, scaling the number of connections to four per via provides for two single-ended signals and two ground segments separating them. In this embodiment, a connector 202 includes a first signal contact 204 and a second signal contact 208 and a pair of ground contacts 204. A via 212 disposed in the printed circuit board 210 includes a first signal segment 214 which mates with contact 204, a second signal segment 218 which mates with contact 208 and a first and second ground segment 216, 220. The pair of ground contacts 204 makes connections to the two opposite segments 216, 220 of the via 212 separating the two signal paths.

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FIGs. 15 and 15A show a variation of this configuration using known connector types, namely eye-of-the-needle pressfit contact 222 and pressure-mount pads 224, with a multi-connection via 212'. The pressfit contact 222 is press fit against segment 223 which provides the required retention force. It should be noted that the architecture shown in FIGs. 15, 15A illustrate a so-called "shielded via" concept which can be applied to existing products, with minor PCB routing redesign.

20

Referring now to FIG. 16, a co-cylindrical waveguide 230 is shown having a similar structure as a co-planer waveguide 250. In the co-cylindrical waveguide 230, an interior wall 234 of a plated hole 232 which is a cylinder includes both a ground conductor 238 and a signal conductor 236. As in a co-planer waveguide 250 having a signal conductor 236' and a ground conductor 238', a signal propagates along the co-cylindrical waveguide 1681 between the signal conductor 236 and the adjacent ground conductor 238.

25

And for $0.173 \leq w/d \leq 1$ or $0 < Z_{l,0} \leq \eta_0/2$:

$$Z_{l,0} = \frac{\pi\eta_0}{4} \left[\ln(2) + 2 \tanh^{-1} \left(\sqrt{\frac{w}{d}} \right) \right]^{-1} \quad \text{Eq. D5}$$

Solving for modulus yields:

$$\frac{w}{d} = \left[\tanh \left(\frac{\pi\eta_0}{8Z_{l,0}} - \frac{\ln(2)}{2} \right) \right]^2 \quad \text{Eq. D6}$$

5

From the latter, the parameters of a co-cylindrical waveguide can be approximated.

It should now be appreciated that a signal can be transmitted on the signal segment 236 and the signal will propagate along the co-cylindrical waveguide as a signal propagate along a co-planar waveguide.

10

Referring now to FIGs. 18A and 18B, having described various embodiments of a via with multiple segments or conductors, it should now be appreciated, an improved multi-connection connector 280 including a plated through hole 282 having at least a first and a second separate electrically isolated segment 262 can be provided with a first surface mount technology contact or pad 256 connected to the first separate electrically isolated segment 262 and a second surface mount technology contact or pad 268 connected to the second separate electrically isolated segment 262.

15

A surface mount device 250 is shown with a plurality of surface mount technology (SMT) contacts 252. A printed circuit board (PCB) 254 includes a multi-connection via (MCV) 260, here including eight separate segments 262, where the surface mount device 250 is mounted. First ones of the segments 262 correspond to ground segments 264 and second ones of the segments 262 correspond to signal segments 266. A plurality of SMT pads 256 are disposed on the printed circuit board 254 and are coupled to predetermined ones of the signal and ground segments 264,

20

25

266 of the MCV 260. The pads 256 are arranged in a pattern which is selected such that when the device 250 is disposed on the PCB 254, the pads 256 are aligned to receive corresponding ones of the SMT contacts 252.

5 Depending upon the particular device 250, all of the contacts 252 can correspond to signal contacts, or all of the contacts can correspond to ground contacts or first ones of the contacts 252 can correspond to signal contacts of the device 250 while second ones of the contacts 252 can correspond to ground contacts of the device 250. The device 250 is oriented with respect to the MCV 260 such that device ground
10 contacts 252 (if any) are coupled to the MCV signal segments 264 and device signal contacts 252 (if any) are coupled to the MCV ground segments 266. Thus the pads 256, are coupled to signal or ground segments of MCV 260 depending upon the function of the device contact which will be coupled thereto. The function of each pad is of course known prior to the manufacture of the PCB in which the MCV 260
15 exists.

 With such an arrangement, a multi-connection connector 280 is provided with a multi-connection via configured as a co-cylindrical waveguide having a similar structure as a co-planer waveguide. In a co-cylindrical waveguide, the interior wall
20 284 of a plated hole 282 which is a cylinder includes both the ground conductors 264 and the signal conductors 266. As in a co-planer waveguide, the signal propagates along between the signal conductor 266 and the adjacent ground conductor 264.

 A co-cylindrical waveguide provides a similar structure and maintains
25 impedance control between signal and ground segments in a way analogous to a co-planar waveguide. Impedance matching is controlled by controlling diameter of the signal segment and signal arch length and gap relative to the ground segment and ground plane clearances. A typical embodiment often results in a small signal segment relative to the ground segment. When appropriate, the ground segment can

bc divided into more than one segment without performance degradation. In the case of one signal segment and one ground segment, the ground segment is typically, but not always, greater than 180 degrees. A differential via structure incorporates two signal segments among the ground segment and typically the signal segment is much narrower than the ground segment. The impedance is matched by controlling diameter, signal segment arch lengths, gap spacing between signal segments, signal segment gap spacing relative to a ground segment and ground plane clearances. By separating signal segments 266 with ground segments 264, multiple signals can be transmitted in a single via. It should be noted that during the manufacturing process the ends of the glass fibers of the printed circuit board 254 may be exposed. The via can be filled with a dielectric material (such as epoxy) to seal the ends of the glass fibers.

It should now be appreciated a different signal can be transmitted on each one of the signal segments 266 and that the surface mount device 250 can be disposed on the printed circuit board 254 with connector 280 utilizing much less surface of the printed circuit board 254 as needed when using known vias.

Referring now to FIGs. 19 and 19A, a pressfit and SMT hybrid connector 300 is shown. A surface mount device 310 is shown with a plurality, here two, of surface mount technology (SMT) contacts 302. A printed circuit board 304 includes a multi-connection via 320, here including four separate segments 322, where the surface mount device 310 is mounted. A plurality, here two, of SMT pads 314 are disposed on the printed circuit board 304 as shown to receive corresponding ones of the SMT contacts 302. A pressfit contact 316 is disposed between the SMT contacts 302 as shown. Here, the pressfit contact 316 provides a ground conductor as well as the required retention force and the SMT contacts 302 provide signal conductors. With such an arrangement, the connector 300 provides a signal path for two signals.

Referring now to FIG. 20, a SMT connector 400 is shown. An SMT by-pass capacitor 410 is shown with two SMT contacts 402. A printed circuit board 404 includes a multi-connection via 420, here including two separate segments 422. Two SMT pads 414 are disposed on the printed circuit board 404 as shown to receive
5 corresponding ones of the SMT contacts 402. Here, one of the separate segments 422 provides a ground conductor and the other one of the separate segments 422 provides a signal conductor or here a power conductor. With such an arrangement, the connector 400 provides a signal path to connect the SMT by-pass capacitor 410 to the printed circuit board 404. In a typical SMT by-pass capacitor, the lead length from the
10 power and ground planes determines the lead inductance. The shorter the lead, the lower the inductance will be, and consequently, the higher the frequency of operation. Utilizing a multi-connection via connector does not change the design of the SMT package of the by-pass capacitor, but takes advantage of the new via geometry for routing only. Placing the via directly below the SMT by-pass capacitor 402, as shown
15 in FIG. 20, reduces the inductance loop to only the surface trace. Because the via itself offers an impedance-controlled structure, the inductance caused by a conventional via configuration does not apply. The offers a superior solution than using micro-vias because power planes most often are located in the middle of the printed wiring board, where micro vias cannot easily reach.

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Referring now to FIGs. 21 and 21A, a printed circuit board 510 is shown to include a plurality of SMT connectors 500 each having a multi-connection via 520 adapted to connect to a daughter board connector, represented here as a collection of SMT wafers 505. It should be appreciated that although MCV 520 is here shown
25 providing connections to a plurality of SMT daughter board wafers, those of ordinary skill in the art will recognize that MCVs 520 may be used to couple any type of PCBs.

Each one of the SMT connectors 500 include an SMT pad 502 to provide a ground connection and an SMT pad 504 to provide a signal connection. In a similar

manner as described earlier, the multi-connection via 520 includes a ground segment 506 to provide a ground conductor connected to a corresponding SMT pad 502 and a signal segment 508 to provide a signal conductor connected to a corresponding SMT pad 504. Each of the SMT pads 502 are connected together with the ground segments 506 as shown.

For each one of the SMT pads 502, an SMT contact 552 is located on the daughter board connector wafer 505 to mate with a corresponding SMT pad 502 as shown to provide a ground connection between the daughter board 505 and the printed circuit board 510. For each one of the SMT pads 504, an SMT contact 554 is located on the daughter board connector wafer 505 to mate with a corresponding SMT pad 504 as shown to provide a signal connection between the daughter board connector wafer 505 and the printed circuit board 510. It should now be appreciated with such an arrangement, when using the SMT connectors 500, fewer vias are required on the printed circuit board 510 to provide a similar number of connections between the daughter board 505 and the printed circuit board 510. The latter provides better routability of signal paths between the daughter boards 505 and the printed circuit board 510. Such an arrangement also provides better signal integrity for high speed circuits i.e. less cross talk, eliminates reflections, reduced attenuation and in general provides better impedance control of the signal path between the daughter board connector wafer 505 and the printed circuit board 510. It should also be appreciated that more connections between the daughter board connectors 505 and the printed circuit board 510 can be made with the SMT connectors 500 within the same amount of space than when using known via structures (assuming that microvias are not being considered).

Referring now to FIGs. 22 and 22A, a printed circuit board 610 is shown to include a plurality of SMT connectors 600 each having a differential multi-connection via 620 for connecting a daughter board connector, represented here as a collection of

SMT wafers 605. It should be noted that connectors shown in FIG. 22 are also described in co-pending application no. 09/198,442 assigned to the assignee of the present invention and incorporated herein by reference.

5 It should be noted that although daughter board connectors are here shown, any type of connector a could also be used. Each one of the SMT connectors 600 include an SMT pad 602 to provide a ground connection and SMT pads 604a and 604b to provide a differential signal connection.

10 The multi-connection via 620 includes a ground segment 606 to provide a ground conductor connected to a corresponding SMT pad 602, a signal segments 608 and 609 to provide a differential signal conductor connected to corresponding SMT pads 604a and 604b. Each of the SMT pads 602 are connected together with the ground segments 606 with other SMT pads 603 disposed between the SMT pads 602
15 as shown.

 The multi-connection via 620 includes two signal conductors providing differential signal path for corresponding signal. For each one of the SMT pads 602, an SMT contact 652 is located on the daughter board connector wafer 605 to mate
20 with a corresponding SMT pad 602 as shown to provide a ground connection between the daughter board connector wafer 605 and the printed circuit board 610. Additionally, an SMT contact 653 located on the daughter board connector wafer 605 provides a ground connection between the daughter board and the printed circuit board 610 mating with SMT pads 603. For each one of the SMT pads 604a, an SMT
25 contact 654 is located on the daughter board connector wafer 605 to mate with a corresponding SMT pad 604a as shown to provide a signal connection between the daughter board connector wafer 605 and the printed circuit board 610. For each one of the SMT pads 604b, an SMT contact 655 is located on the daughter board connector wafer 605 to mate with a corresponding SMT pad 604b as shown to provide

a signal connection between the daughter board 605 and the printed circuit board 610.

5 It should now be appreciated with such an arrangement, when using the SMT connectors 600, fewer vias are required on the printed circuit board 610 to provide a similar number of connections between the daughter board 605 and the printed circuit board 610. The latter provides better routability of signal paths between the daughter boards connector wafer 605 and the printed circuit board 510 as well as routability between rows, which is not possible with conventional vias. It should also be
10 appreciated that conventional via structures do not provide a true differential connection between layers in the PCB, thus this arrangement provides a superior performing connection from the daughter card connector to the layer trace.

Referring now to FIG. 23, an alternative embodiment of printed circuit board
15 610 is shown to include a plurality of SMT connectors 600' each having a multi-connection via 620 provided in the printed circuit board 610. In the alternative embodiment, an additional via 670 connected to a pad 671 is included to provide a ground connection and replacing the surface traces of the previous embodiment. It should be noted that the embodiment of FIG. 23 is similar to the same differential
20 configuration as the embodiments of FIGs. 21-22 but instead of a surface trace connecting the additional ground pin (specific to the connector illustrated) a separate conventional ground via is used.

In present vias, the metal plating of the via acts to seal the cut drilled surface
25 of the via. In fabricating multi-connection vias, drilling exposes cut ends of the glass fiber of the printed wiring board, allowing the printed circuit board to absorb moisture and other chemicals. Cutting the plating to form a split via exposes the fibers again. In all of the embodiments showing a multi-connection via, the via can be filled with a dielectric material (such as epoxy) to seal the ends of the glass fibers exposed between

the conducting material. For pressfit contacts a soft gel seal can be used which will push out of the way of the connector as it is pressed into the hole to seal the ends of the glass fibers exposed between the conducting material.

5 It should now be appreciated that various connectors can be contemplated, for example, referring now to FIGs. 2 - 3E any one of the multi-connection vias shown could be adapted to provide an appropriate multi-connection connector.

10 It should be appreciated that multi-connection vias, described herein, provide a structure and method for matching the impedance of vertical and in-plane features by forming co-cylindrical waveguides. Solutions from a high-frequency full-wave solver provide insight into field interactions within multi-connection vias; and results from these simulations and signal integrity experiments indicate impedance "tuneability" by adjusting the multi-connection via dimensions. The results also suggest that features
15 can be impedance-matched independent of via diameter.

 All references cited herein are hereby incorporated herein by reference in their entirety.

20 Having described preferred embodiments of the invention, it will now become apparent to one of ordinary skill in the art that other embodiments incorporating their concepts may be used. It is felt therefore that these embodiments should not be limited to disclosed embodiments, but rather should be limited only by the spirit and scope of the appended claims.

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What is claimed is:

Claims

- 1 1. An interconnection structure for providing a signal path between a first layer
2 and a second different layer of a multi-layer structure, the interconnection structure
3 comprising a plated through hole having a plurality of electrically isolated segments
4 with at least one of the plurality of electrically isolated segments coupled to one of a
5 signal path and a circuit component and at least one of the electrically isolated
6 segments coupled to a ground plane layer of the multi-layer structure.
- 1 2. The interconnection structure of Claim 1 wherein each of the plurality of
2 electrically isolated segments coupled to signal paths are provided having equal
3 widths and each of the at least one of the electrically isolated segments coupled to
4 ground are provided having equal widths.
- 1 3. The interconnection structure of Claim 1 wherein at least two of the plurality
2 of electrically isolated segments are coupled to signal paths and are provided having
3 different widths.
- 1 4. The interconnection structure of Claim 1 wherein at least two of the plurality
2 of electrically isolated segments are coupled to the ground plane layer of said multi-
3 layer structure and are provided having different widths.
- 1 5. The interconnection structure of Claim 1 wherein the at least one of the
2 plurality of electrically isolated segments which is coupled to a signal path has a width
3 which is less than the width of the at least one of the electrically isolated segments
4 coupled to the ground plane layer of said multi-layer structure.

1 6. The interconnection structure of Claim 1 wherein said plurality of electrically
2 isolated segments of said plated through hole are disposed in a symmetric pattern
3 about a central longitudinal axis of said plated through hole.

1 7. The interconnection structure of Claim 1 wherein said plurality of electrically
2 isolated segments of said plated through hole are disposed in an asymmetric pattern
3 about a central longitudinal axis of said plated through hole.

1 8. The interconnection structure of Claim 1 wherein said plated through hole is
2 provided having a cross-sectional shape which is substantially round.

1 9. The interconnection structure of Claim 1 wherein said plated through hole is
2 provided having a cross-sectional shape which is substantially rectangular.

1 10. The interconnection structure of Claim 3 wherein said plated through hole is
2 provided having a cross-sectional shape which is substantially square.

1 11. The interconnection structure of Claim 1 wherein said plated through hole is
2 provided having an irregular cross-sectional shape.

1 12. The interconnection structure of Claim 1 wherein each of the plurality of
2 electrically isolated segments are provided having substantially equal widths.

1 13. A interconnection structure for providing a signal path between a first signal
2 trace on a first layer of a multi-layer structure and a second signal trace on a second
3 different layer of the multilayer structure, the interconnection structure comprising:
4 (a) a first electrically conductive path extending in a substantially vertical
5 direction along a surface of an opening in the multi-layer structure between the first
6 layer and the second layer of the multi-layer structure; and

7 (b) a second electrically conductive path extending in a substantially vertical
8 direction along the surface of the opening in the multi-layer structure between the first
9 layer and the second layer of the multi-layer structure and electrically isolated from
10 the first electrically conductive path, wherein a first one of the first and second
11 electrically conductive paths is coupled to the first and second signal traces and a
12 second one of the first and second electrically conductive paths is coupled to a
13 reference potential.

1 14. The interconnection structure of Claim 13 wherein the arc lengths of the first
2 and second electrically conductive paths are selected such that the interconnection
3 structure is provided having a predetermined electrical impedance characteristic.

1 15. The interconnection structure of Claim 14 wherein the multi-layer structure
2 includes a plurality of ground plane layers each of the which is provided from a
3 conductive material a portion of which has been removed from the region of the
4 ground plane layer proximate the location of the one of the electrically conductive
5 paths coupled to the first and second signal traces.

1 16. The interconnection structure of Claim 15 wherein the ground plane layer is
2 provided having conductive material in an asymmetrical pattern around the one of the
3 electrically conductive paths coupled to the first and second signal traces.

1 17. The interconnection structure of Claim 13 further wherein the first electrically
2 conductive path is coupled to the first and second signal traces, the second electrically
3 conductive path is coupled to ground and the interconnection structure further
4 comprises a third electrically conductive path extending in a substantially vertical
5 direction between the first layer and the second layer of the multilayer structure and is
6 coupled to third and fourth signal traces of the multi-layer structure.

1 18. A circuit comprising:
2 a first plurality of multi-connection vias arranged to provide a first cluster of
3 signal connection regions, each of the first plurality of multi-connection vias having at
4 least one segment coupled to ground; and
5 a second plurality of multi-connection vias arranged to provide a second
6 cluster of signal connection regions, each of the second plurality of multi-connection
7 vias having at least one segment coupled to ground and wherein said second plurality
8 of multi-connection vias are disposed in relation to said first plurality of multi-
9 connection vias to define a plurality of distinct routing channels between the first and
10 second clusters of signal connection regions.

1 19. The circuit of Claim 18 wherein:
2 the first plurality of multi-connection vias are disposed such that the ground
3 segments are juxtaposed; and
4 the second plurality of multi-connection vias are disposed such that the ground
5 segments are juxtaposed.

1 20. The circuit of Claim 18 wherein at least some of said first and second plurality
2 of multi-connection vias are provided as differential multi-connection vias having a
3 first pair of signal segments adapted to coupled to a first differential pair of signal
4 paths and a second pair of signal segments adapted to couple to a second differential
5 pair of signal paths wherein said first pair of signal paths are on a first layer of a multi-
6 layer printed circuit board and the second pair of signal paths are on a second different
7 layer of the multi-layer printed circuit board.

1 21. The circuit of Claim 18 wherein at least some of said first plurality of multi-
2 connection vias have a plurality of signal segments.

1 22. The circuit of Claim 18 wherein at least at least some of said first plurality of
2 multi-connection vias have a plurality of signal segments and a plurality of ground
3 segments.

1 23. The interconnection structure of Claim 1 further comprising at least one pad
2 coupled to each of said plurality of electrically isolated segments wherein each of said
3 pads is provided having one of a radial shape or a parallel shape.

1 24. A multi-connection via provided in a printed circuit board having a plurality of
2 signal layers and a plurality of ground layers, the multi-connection via comprising a
3 plated through hole provided in the printed circuit board, said plated through hole
4 having a first plurality of separate electrically isolated segments, with at least one of
5 the first plurality of electrically isolated segments adapted to coupled to one of a
6 signal path and a circuit component and at least one of the first plurality of electrically
7 isolated segments adapted to couple to at least one of the plurality of ground plane
8 layers of the printed circuit board, wherein the widths of each of the at least one of the
9 plurality of electrically isolated segments adapted to coupled to one of a signal path
10 and a circuit component and the at least one of the electrically isolated segments
11 adapted to couple to at least one of the plurality of ground plane layers of the printed
12 circuit board are selected to provide the multi-connection via having a predetermined
13 impedance characteristic.

1 25. The multi-connection via of Claim 24 wherein said plated through hole has a
2 first segment corresponding to a first signal segment which is adapted to couple to a
3 first signal trace and a second segment corresponding to a first ground segment which
4 is adapted to couple to one of the plurality of ground plane layers of the printed circuit
5 board.

1 26. The multi-connection via of Claim 25 wherein the first signal segment is a first
2 one of a plurality of signal segments and the first ground segment is a first one of a
3 plurality of ground segments.

1 27. The multi-connection via of Claim 25 further comprising a second signal
2 segment wherein said first and second signal segments are adapted to receive a
3 differential signal pair.

1 28. The multi-connection via of Claim 27 wherein the first and second signal
2 segments correspond to first ones of a plurality of pairs of differential signal segments.

1 29. The multi-connection via of Claim 24 further comprising a second plurality of
2 separate electrically isolated segments provided in said plated through hole, with at
3 least one of the second plurality of electrically isolated segments adapted to coupled to
4 at least one the ground plane layers of the printed circuit board.

1 30. The multi-connection via of Claim 29 wherein the first plurality of separate
2 electrically isolated segments are disposed in said plated through hole above said
3 second plurality of separate electrically isolated segments such that first ends of the
4 first plurality of separate electrically isolated segments are spaced by a predetermined
5 distance from second ends of the second plurality of separate electrically isolated
6 segments.

1 31. The multi-connection via of Claim 24 wherein each of said first plurality of
2 segments are provided having a split around a circumferential axis of said plated
3 through hole to provide the multi-connection via having first and second multi-
4 connection via portions.

1 32. A interconnection device for providing a signal path between a first layer and a
2 second different layer of a multilayer structure, the interconnection device comprising
3 a plated through hole having a first continuous nonconductive region provided therein
4 to define a first region of the plated through hole corresponding to a via trace segment
5 and a second region of the plated through hole corresponding to a ground trace
6 segment wherein said via trace segment is electrically isolated from the ground trace
7 segment and is adapted to couple to a signal path.

1 33. The interconnection device of Claim 32 wherein said signal path traverses in a
2 direction which is not vertical with respect to a central longitudinal axis of the via.

1 34. The interconnection device of Claim 32 wherein the first continuous
2 nonconductive region is a first one of a plurality of continuous nonconductive regions,
3 each of said plurality of continuous nonconductive regions defining a like plurality of
4 regions in the plated through hole corresponding to via trace segments wherein each
5 of said plurality of via trace segments are electrically isolated from the ground trace
6 segment and each of said plurality of via trace segments are adapted to couple to a
7 signal path.

1 35. An interconnection structure for providing a signal path between a first layer
2 and a second different layer of a multi-layer structure which includes a plurality of
3 signal layers and a plurality of ground layers, the interconnection structure
4 comprising:

5 a plated through hole having a first end, a second end and a plurality of
6 electrically isolated segments extending from the first end of the plated through hole
7 to the second end of the plated through hole with at least one of the plurality of
8 electrically isolated segments coupled to at least one of the plurality of signal layers of
9 the multi-layer structure and at least one of the electrically isolated segments coupled
10 to at least one of the plurality of ground layers of the multi-layer structure;

11 a first layer disposed over the first end of the plated through hole such that the
12 first end of the plated through hole is not exposed through the first layer; and
13 a second layer disposed over the second end of the plated through hole such
14 that the second end of the plated through hole is not exposed through the second layer.

1 36. The multilayer structure of Claim 36 wherein the widths of each of the
2 plurality of electrically isolated segments is selected such that the segments coupled to
3 signal layers are provided having a predetermined impedance characteristic.

1 37. The multilayer structure of Claim 36 wherein at least some of the plurality of
2 electrically isolated segments are coupled to a pad on one of the signal or ground
3 layers of the multi-layer structure.

1 38. The multilayer structure of Claim 35 wherein said plated through hole includes
2 a surface corresponding to exposed portions of a dielectric and said plated through
3 hole is filled with a material which reduces the amount of moisture absorbed by the
4 exposed portions of the dielectric in said plated through hole.

1 39. A multilayer structure comprising:
2 a plurality of ground layers;
3 a plurality of signal layers;
4 a first signal trace disposed on a first layer of said plurality of signal layers;
5 a second signal trace disposed on a second different layer of said plurality of
6 signal layers;
7 a plurality of support layers for structurally supporting said plurality of signal
8 layers and ground layers;
9 a multi-connection via having a first ground segment coupled to one of said
10 plurality of ground plane layers, a first signal segment having first portion coupled to
11 said first signal trace and having a second portion coupled to said second signal trace.

1 40. The multi-layer structure of Claim 39 further comprising a third signal trace
2 disposed on a third layer of said plurality of signal layers and a fourth signal trace
3 disposed on a fourth layer of said plurality of signal layers and wherein said a multi-
4 connection via includes a second ground segment coupled to one of said plurality of
5 ground plane layers and a second signal segment having a first portion coupled to said
6 third signal trace and having a second portion coupled to said fourth signal trace.

1 41. The structure of Claim 40 wherein said first and second signal segments and
2 said first and second ground segments of said multi-connection via are
3 disposed in a symmetric pattern about a longitudinal central axis of said multi-
4 connection via.

1 42. The multi-layer structure of Claim 41 wherein said first and second signal
2 traces are orthogonally disposed with respect to said multi-connection via.

1 43. The multi-layer structure of Claim 41 wherein said first and second signal
2 traces are aligned along a horizontal axis through said multi-connection via.

1 44. A circuit comprising:
2 a multilayer structure having a multi-connection via, said multi-connection via
3 having first and second electrically isolated segments and a predetermined spacing
4 between the first and second segments; and
5 a connector having first and second contacts spaced by a predetermined
6 distance and adapted to be disposed in said multi-connection via, said first and second
7 contacts are disposed against the first and second segments of said multi-connection
8 via.

1 45. The circuit of Claim 44 wherein:

2 said connector is provided having at least one ground conductor and a plurality
3 of signal conductors; and

4 said multi-connection via includes at least one ground segment and a like
5 plurality of electrically isolated signal segments, wherein the signal segments are
6 provided having a size and spacing adapted to coupled to the plurality of signal
7 conductors of said connector.

1 46. The circuit of Claim 44 wherein

2 said connector is provided having an eye-of-the- needle connector disposed in
3 the multi-connection via such that a first portion of the eye of needle connector
4 contacts a first electrically isolated segment of the multi-connection via and a second
5 portion of the eye of needle connector contacts a second different electrically isolated
6 segment of the multi-connection via.

1 47. The circuit of Claim 46 wherein the first electrically isolated segment of the
2 multi-connection via is coupled to ground and the second different electrically isolated
3 segment of the multi-connection via is coupled to a signal line.

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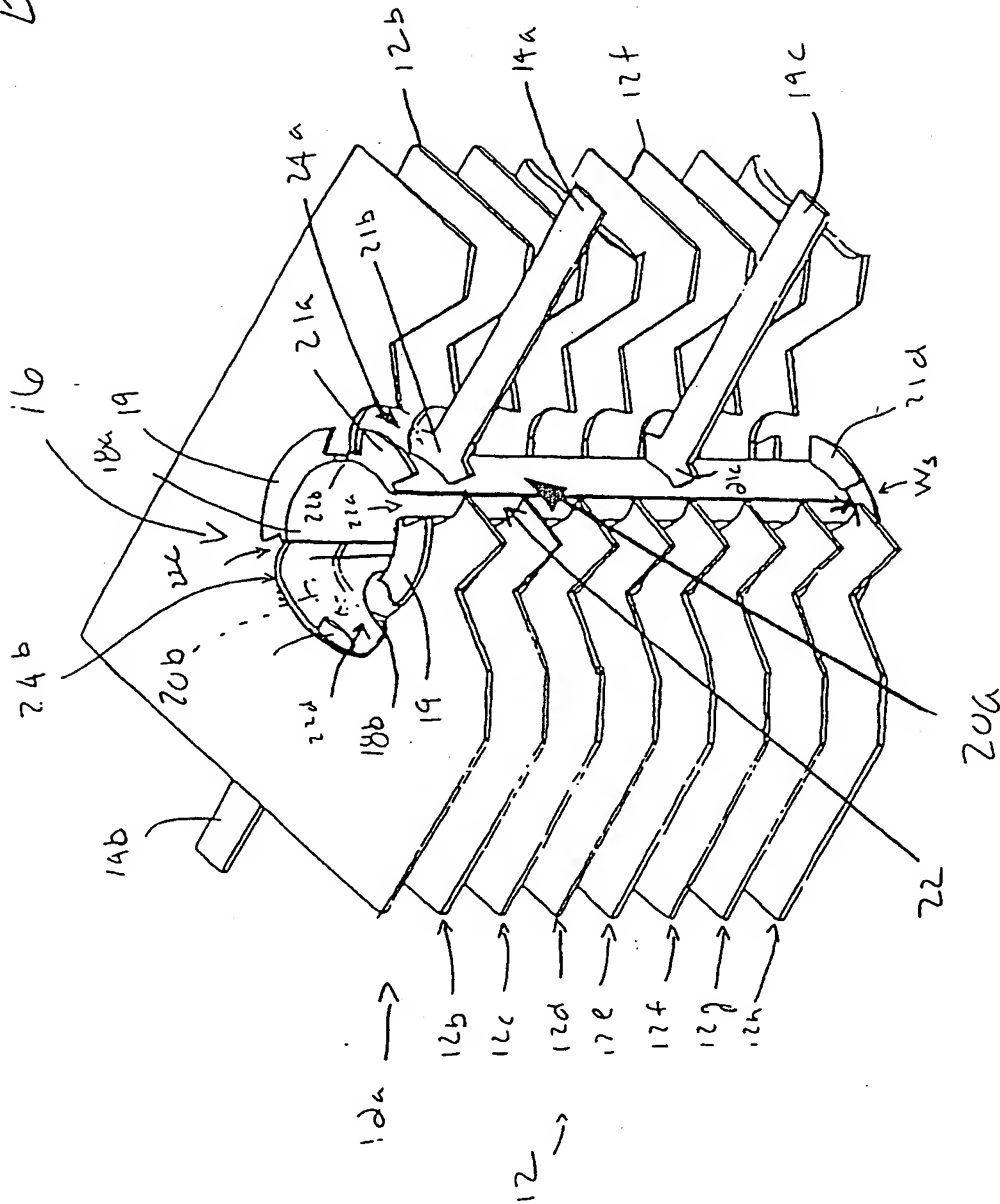
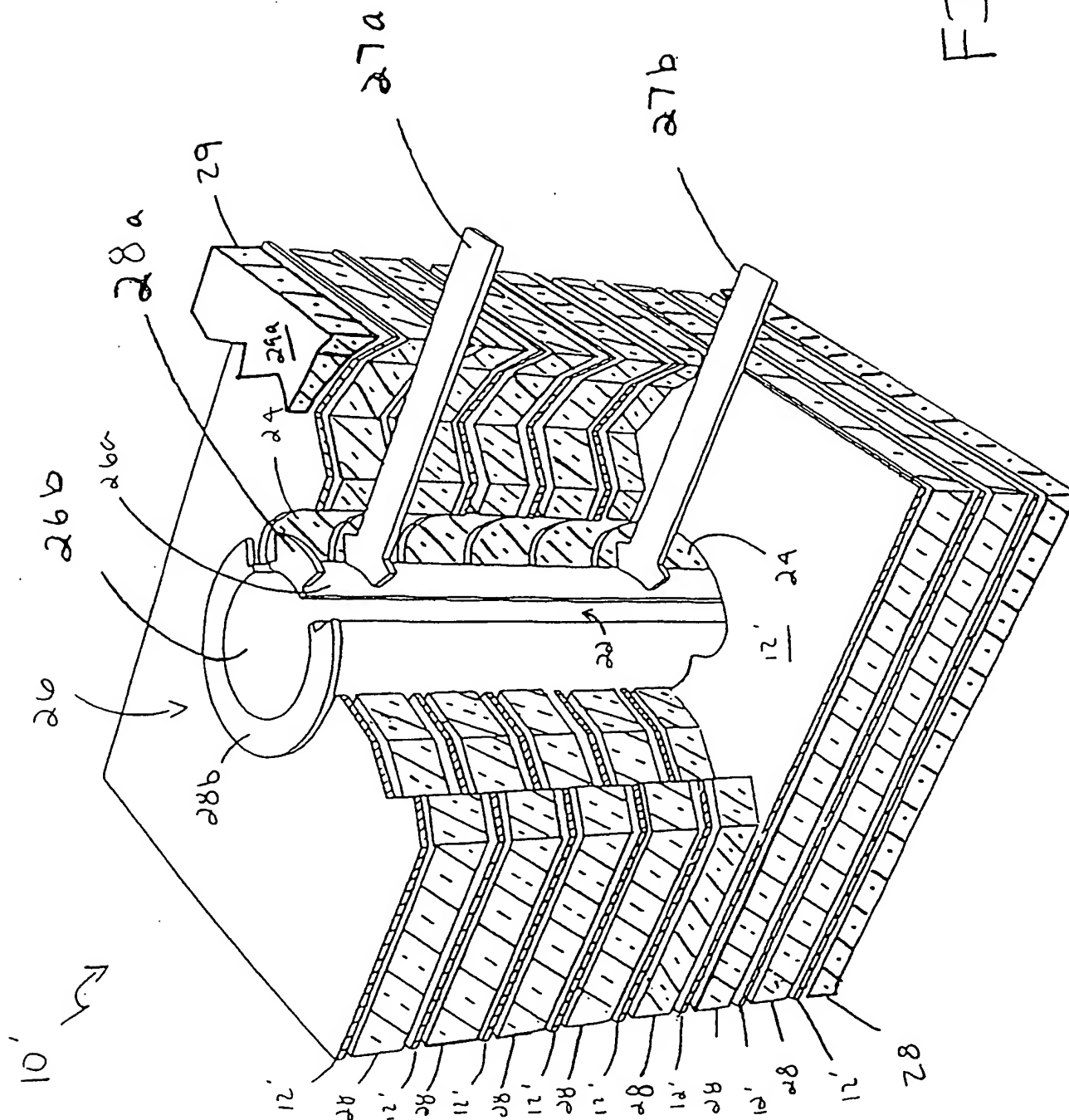
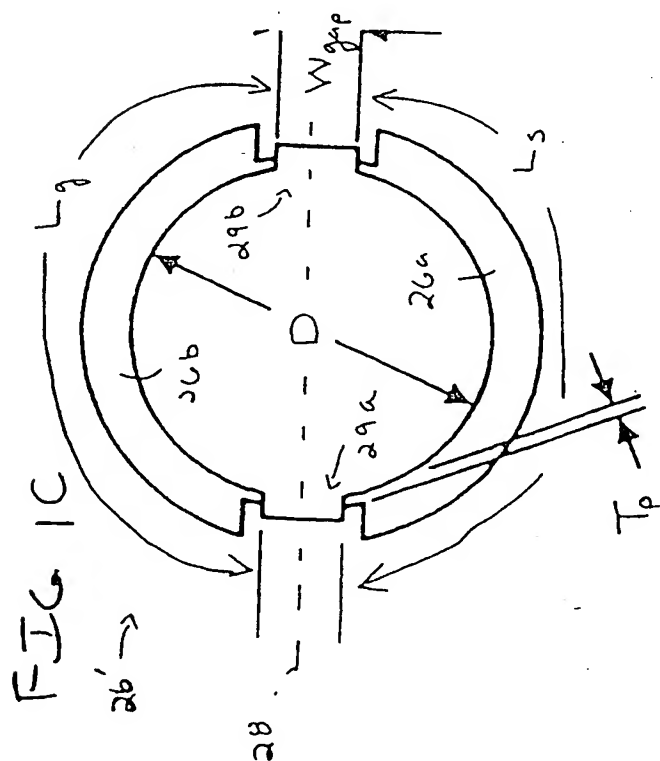
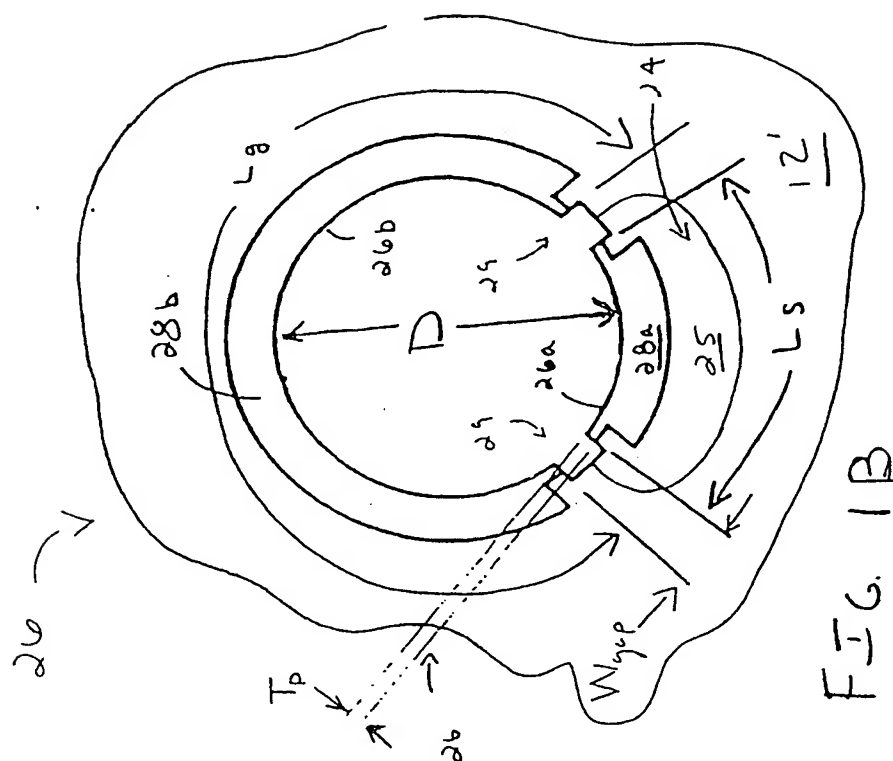


FIG. 1





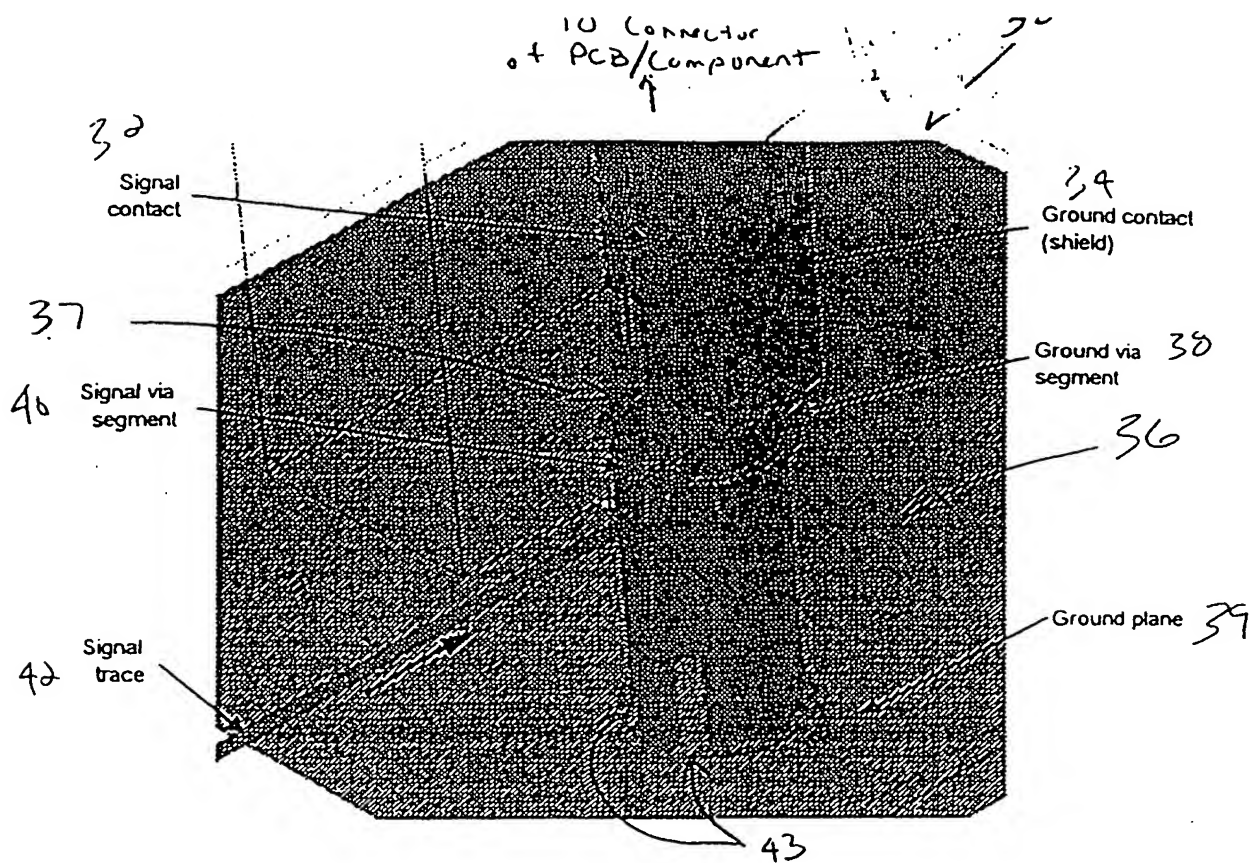


FIG. 1D

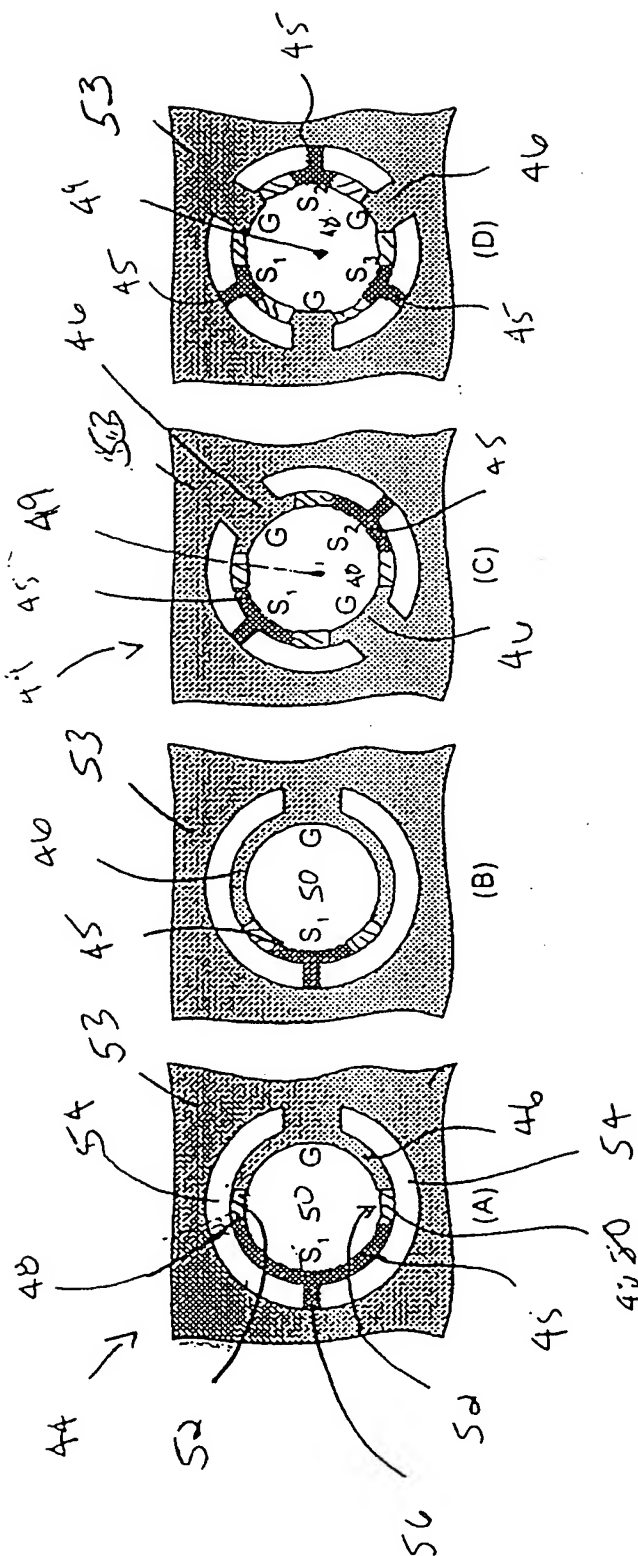


FIG. 2

FIG. 2A

FIG. 2B

FIG. 2C

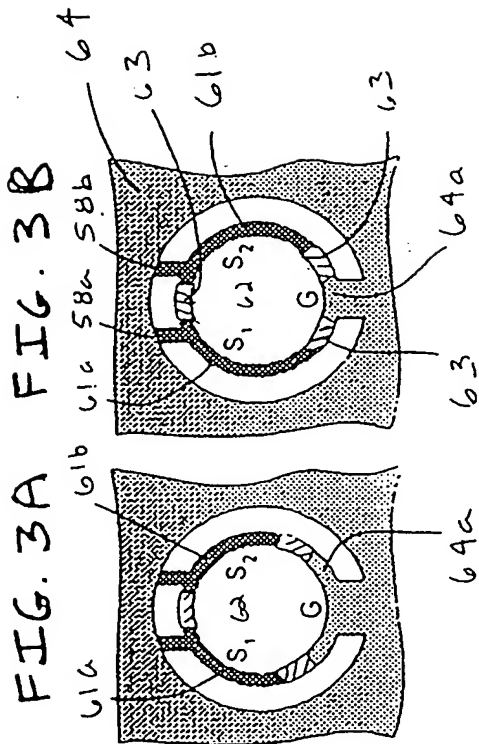
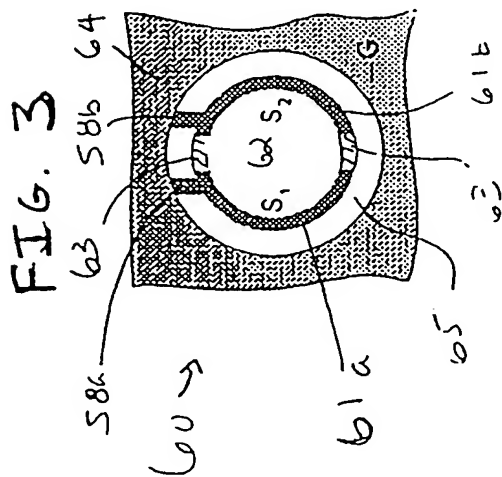


FIG. 3B

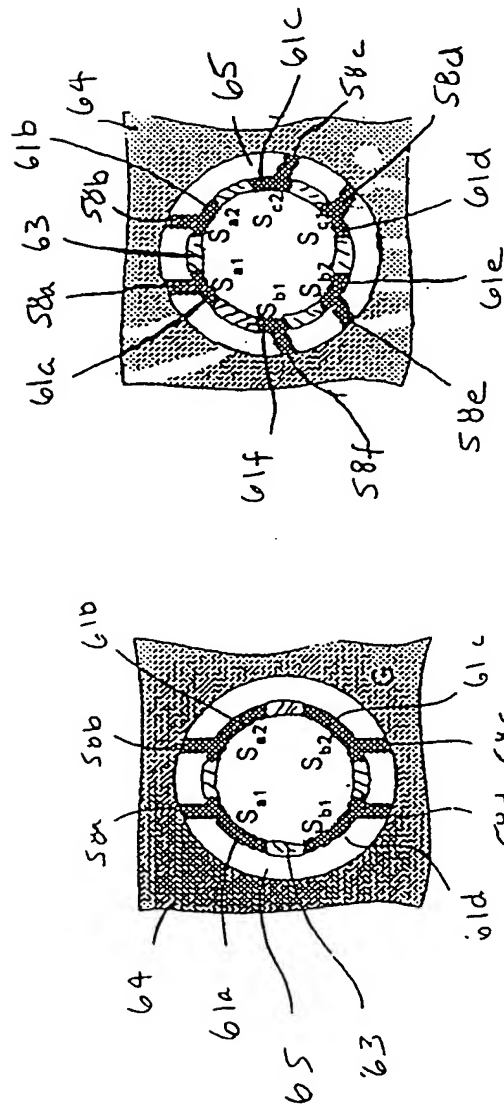
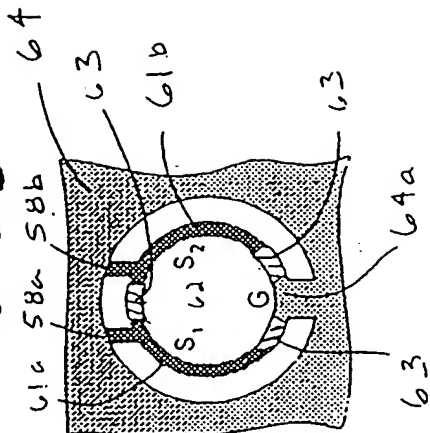


FIG. 3C

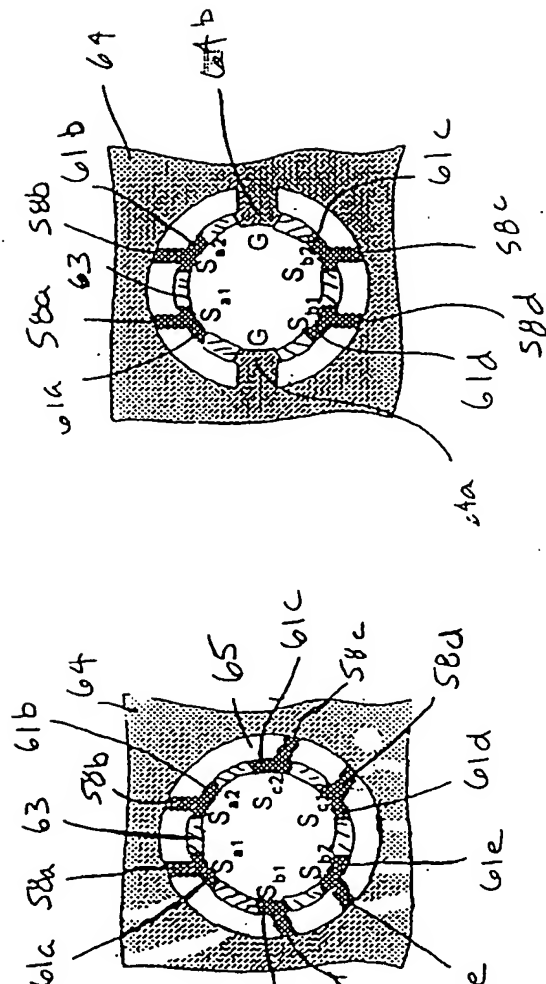


FIG. 3D

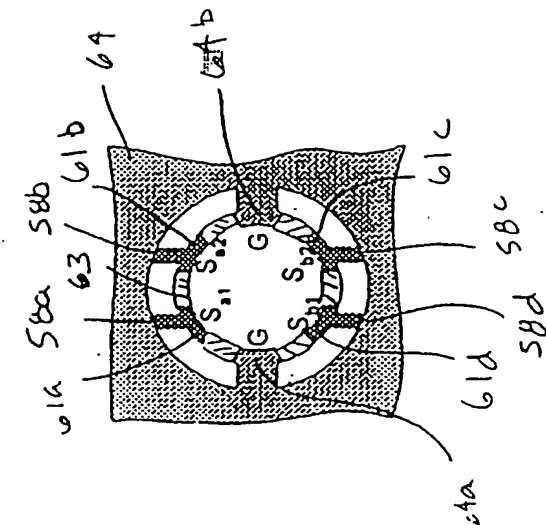


FIG. 3E

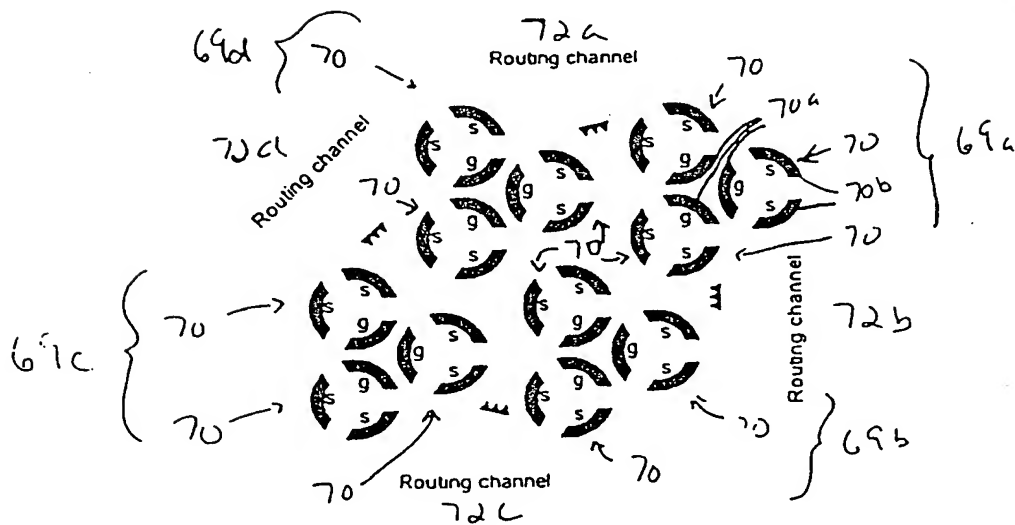
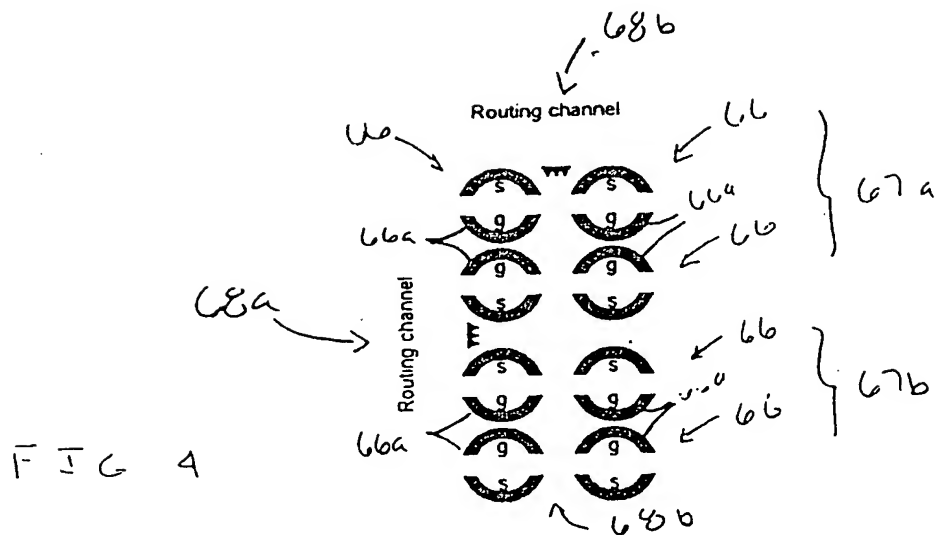
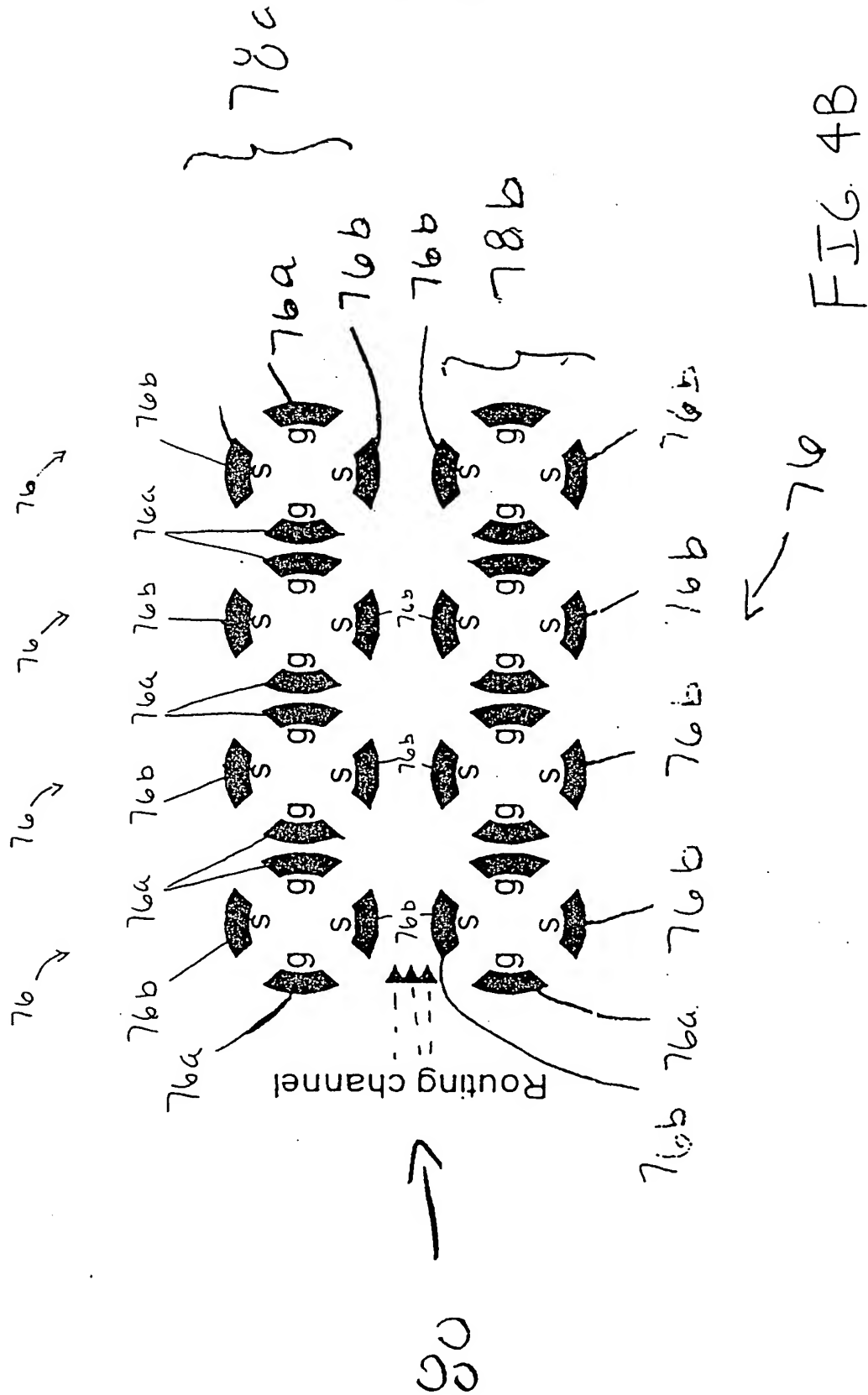


FIG 4A



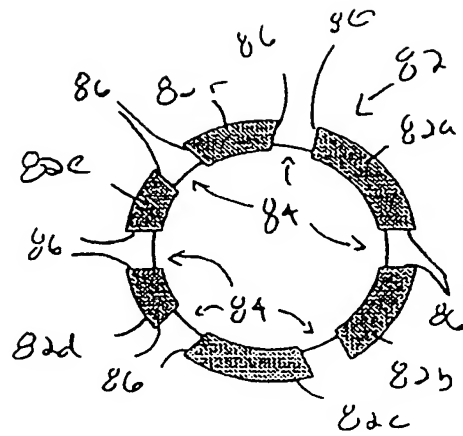


FIG. 5

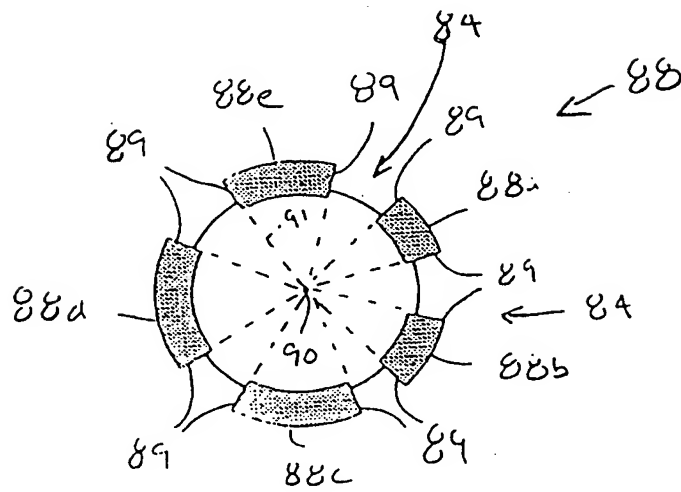


FIG. 6

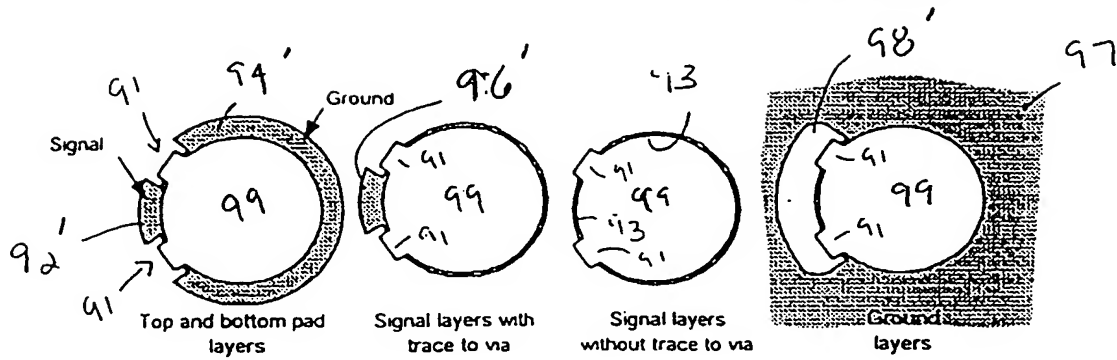
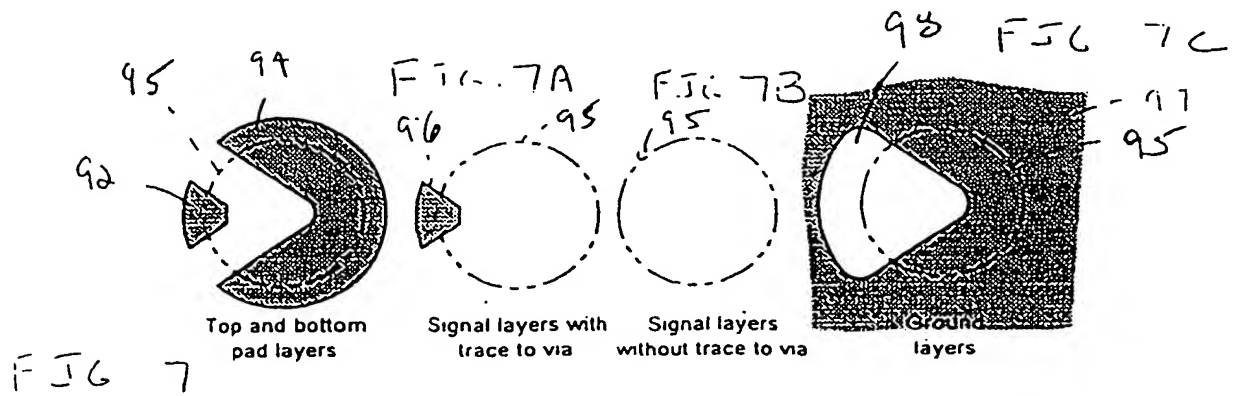


FIG. 8

FIG. 8A

FIG. 8B

FIG. 8C

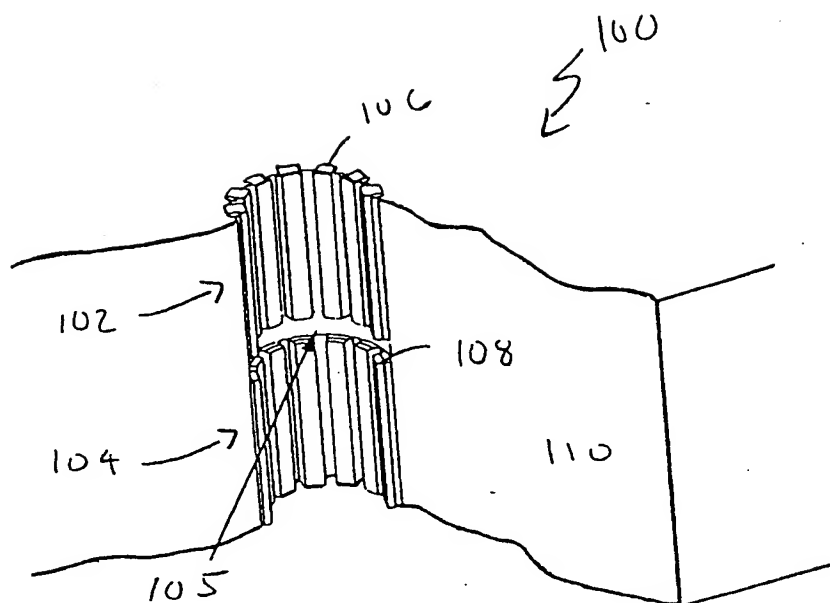


FIG. 9

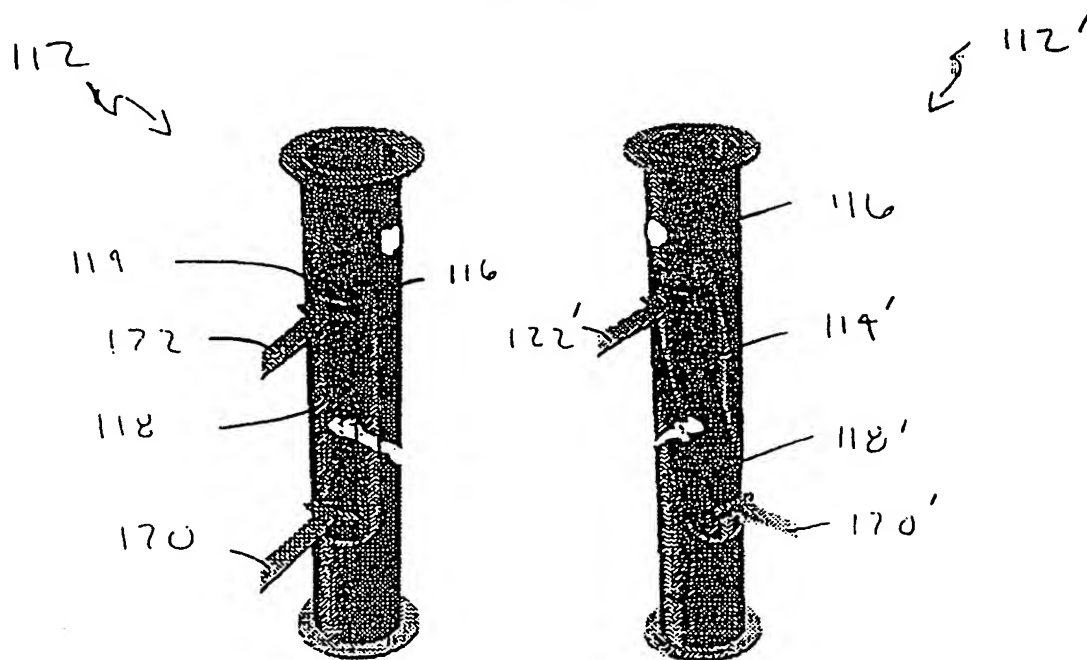


FIG 10

FIG 10A

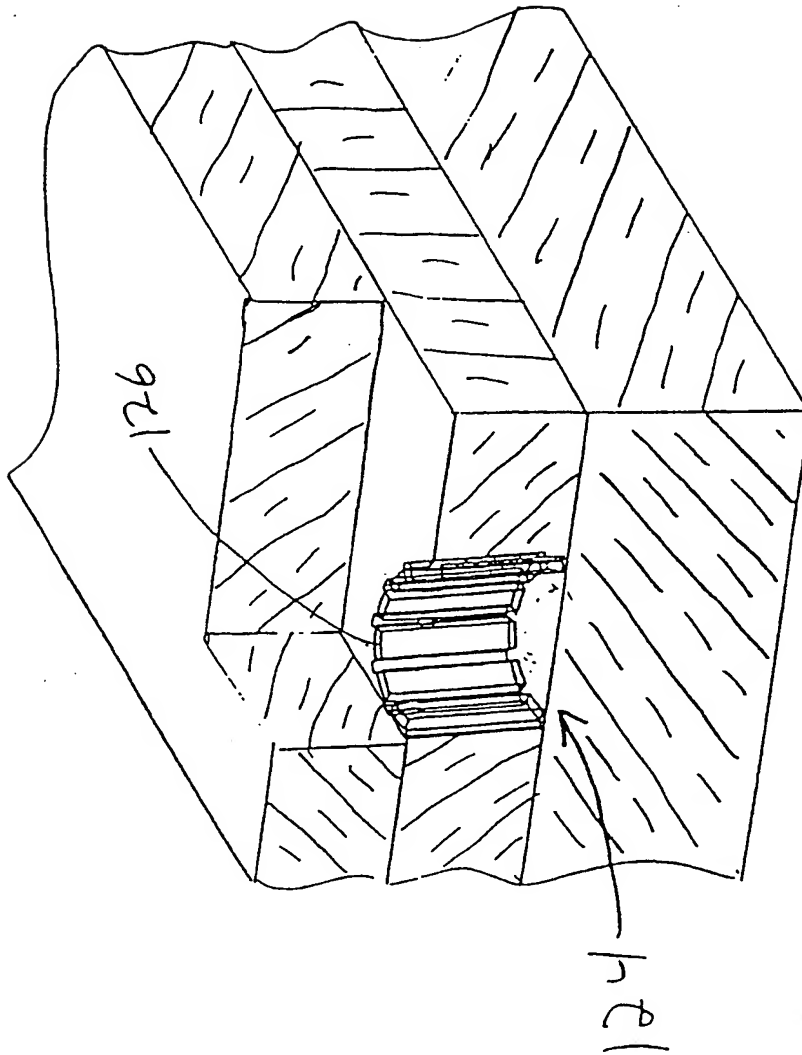


FIG. 11

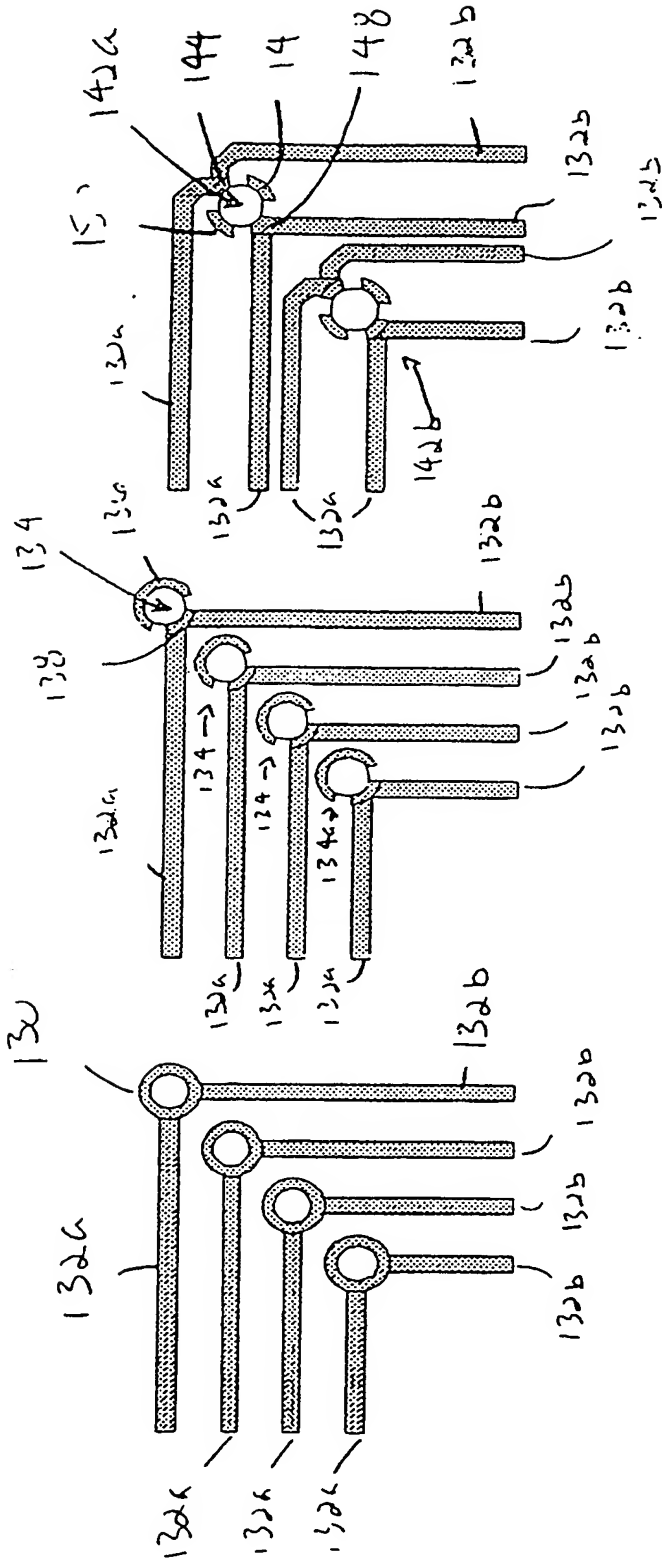


FIG 12

FIG. 12A

FIG. 12B

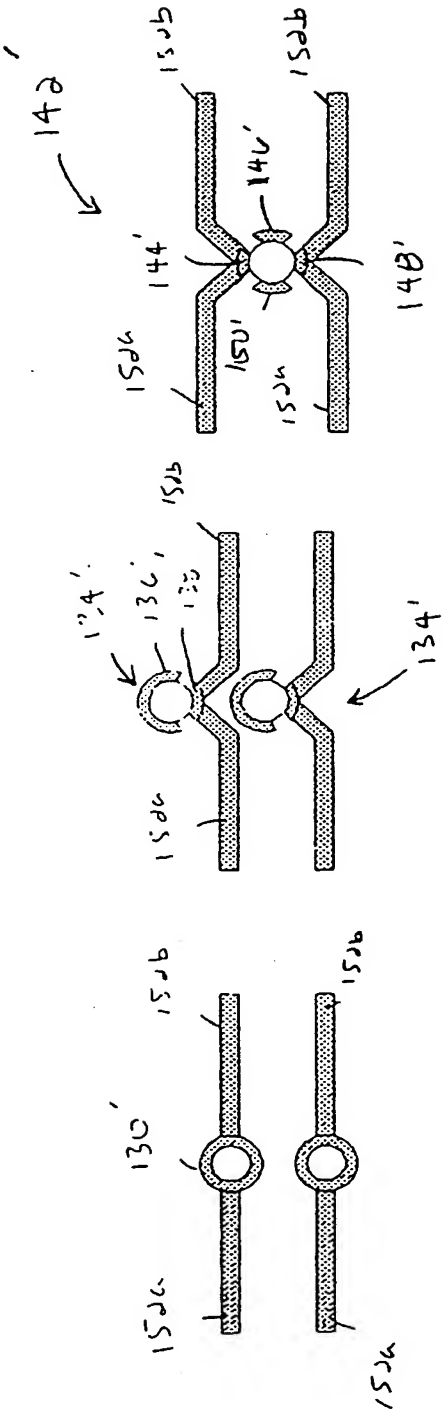


FIG. 12E

FIG 12D

FIG 12C

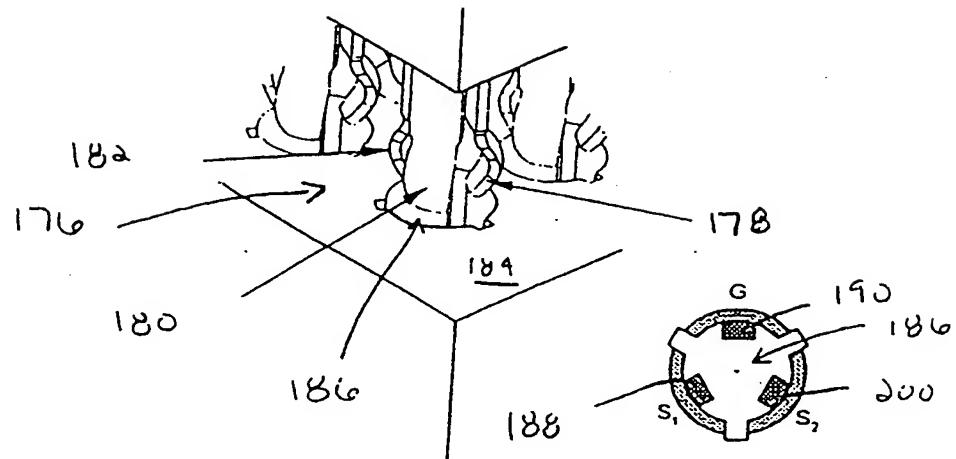


FIG. 13D

F I G. 13 C

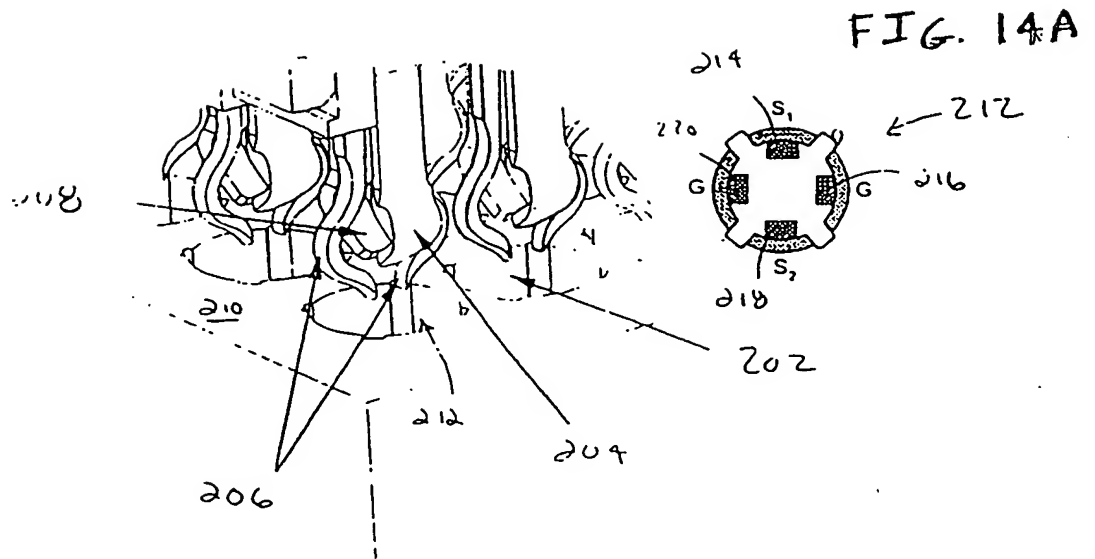


FIG 14

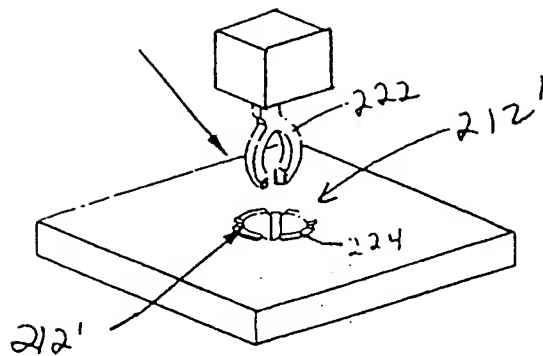


FIG. 15

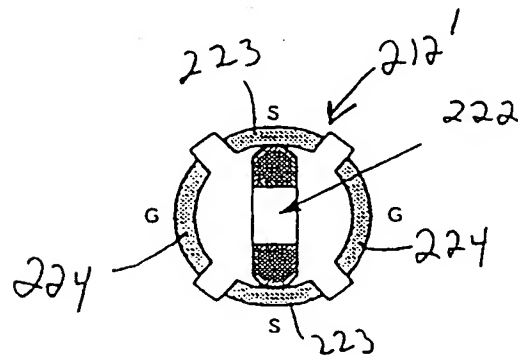
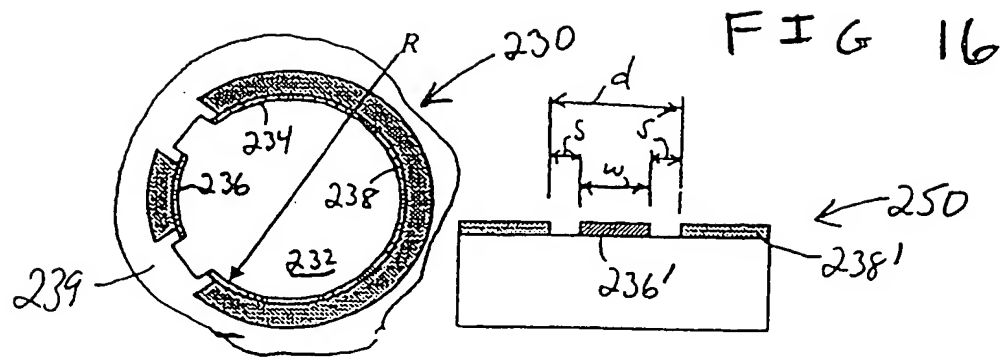


FIG. 15A



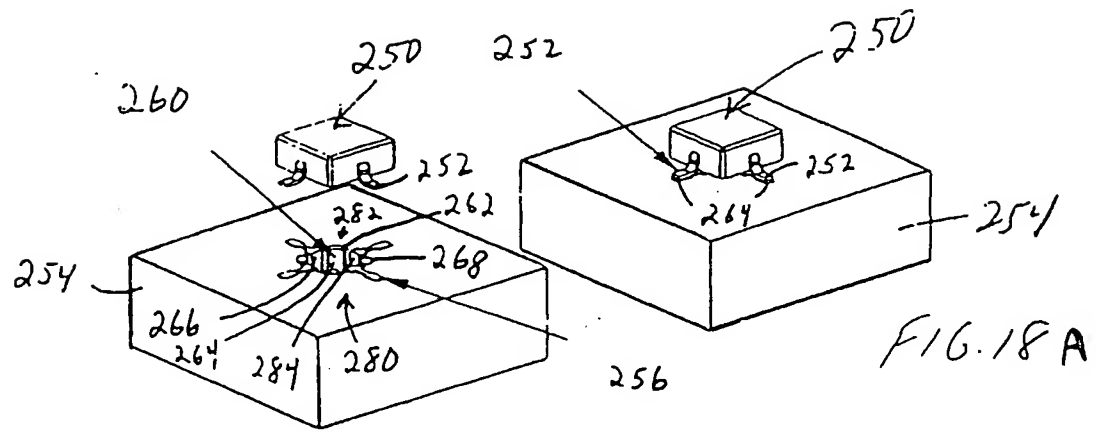
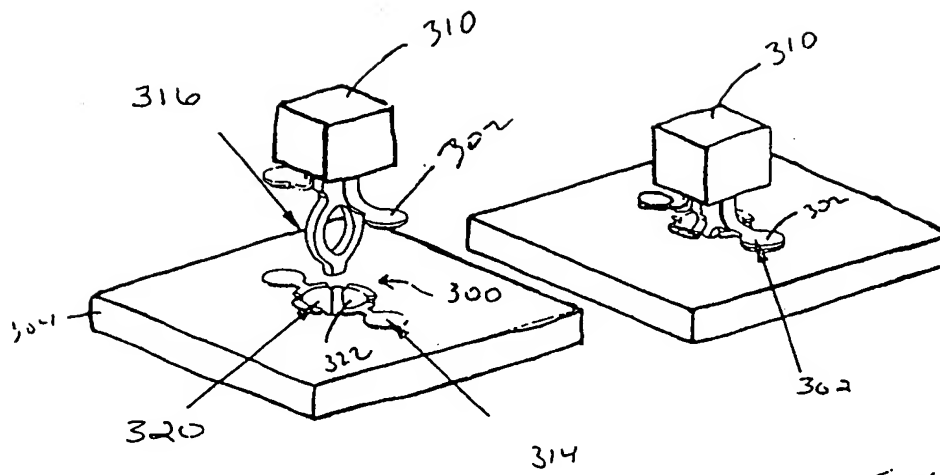


FIG. 18



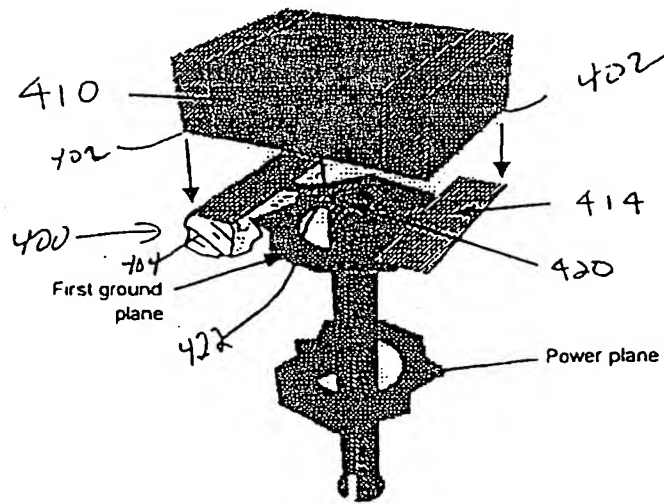
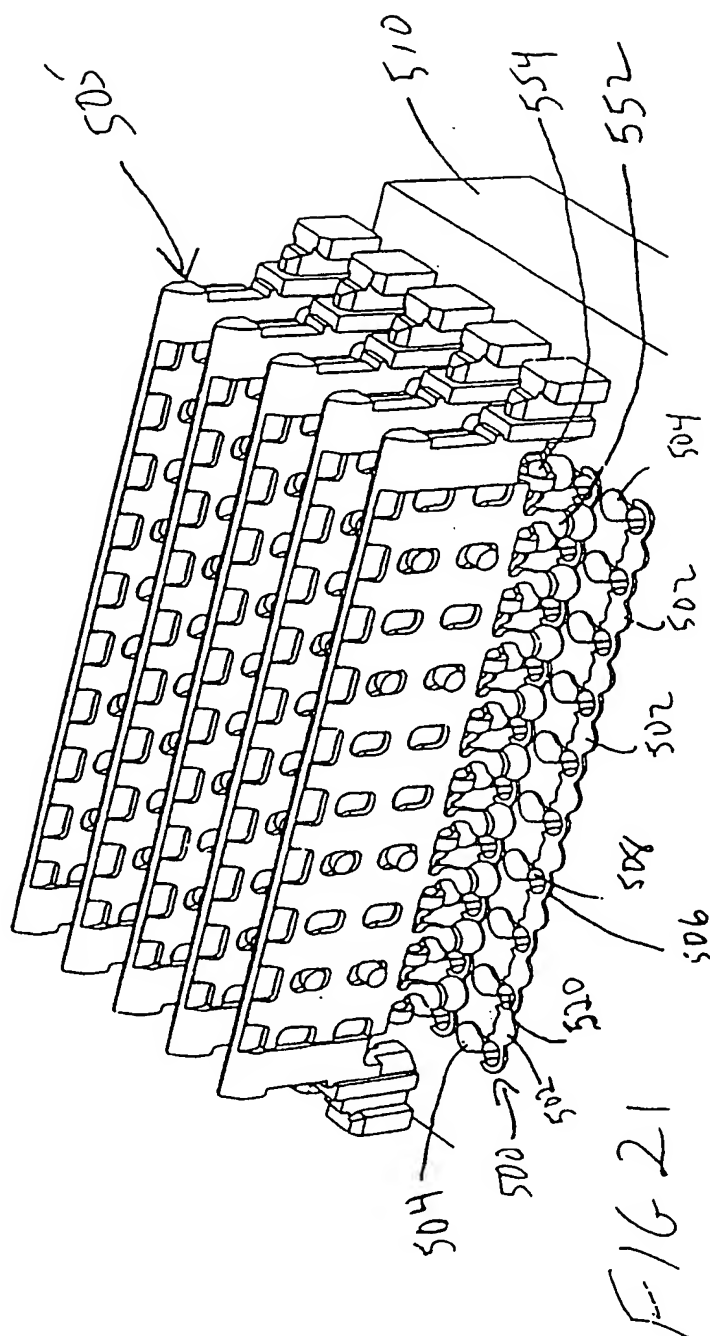


FIG. 20



SCALE 10.00

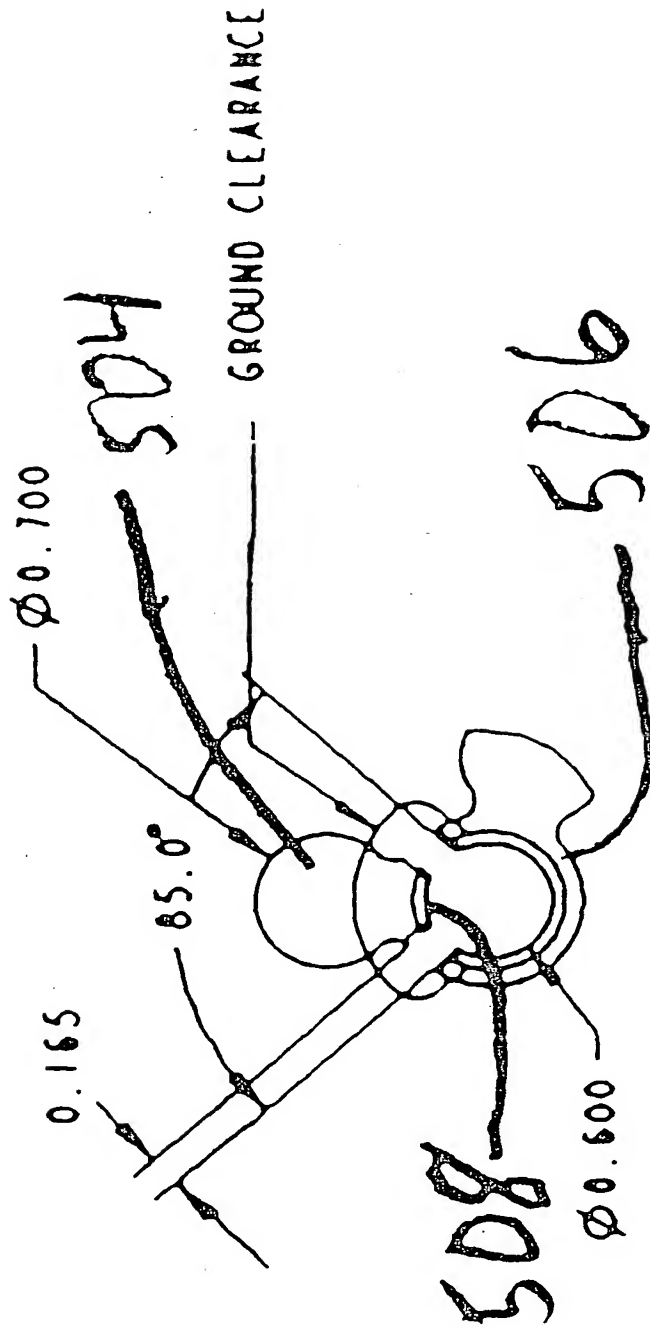
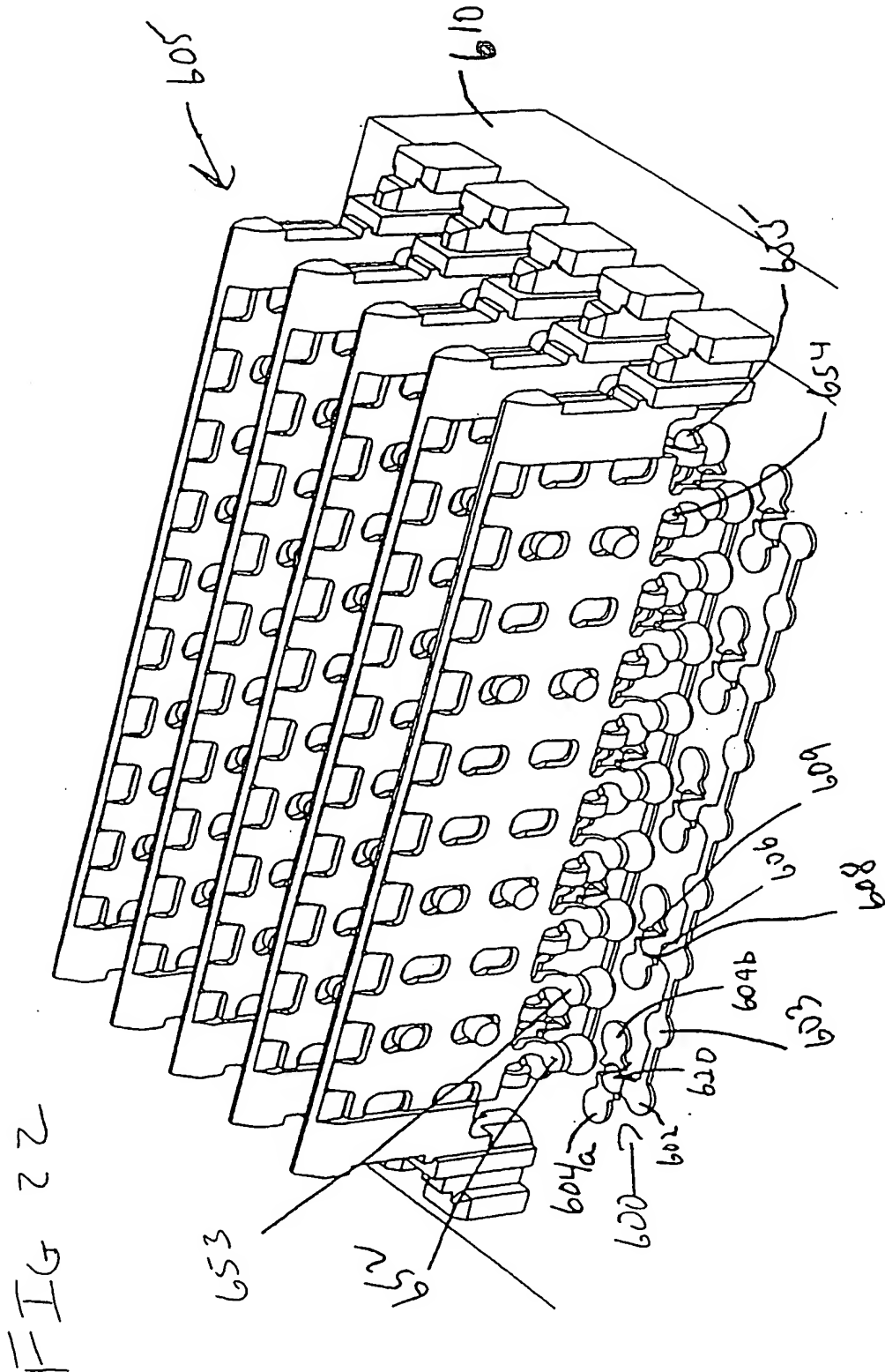


FIG 21A



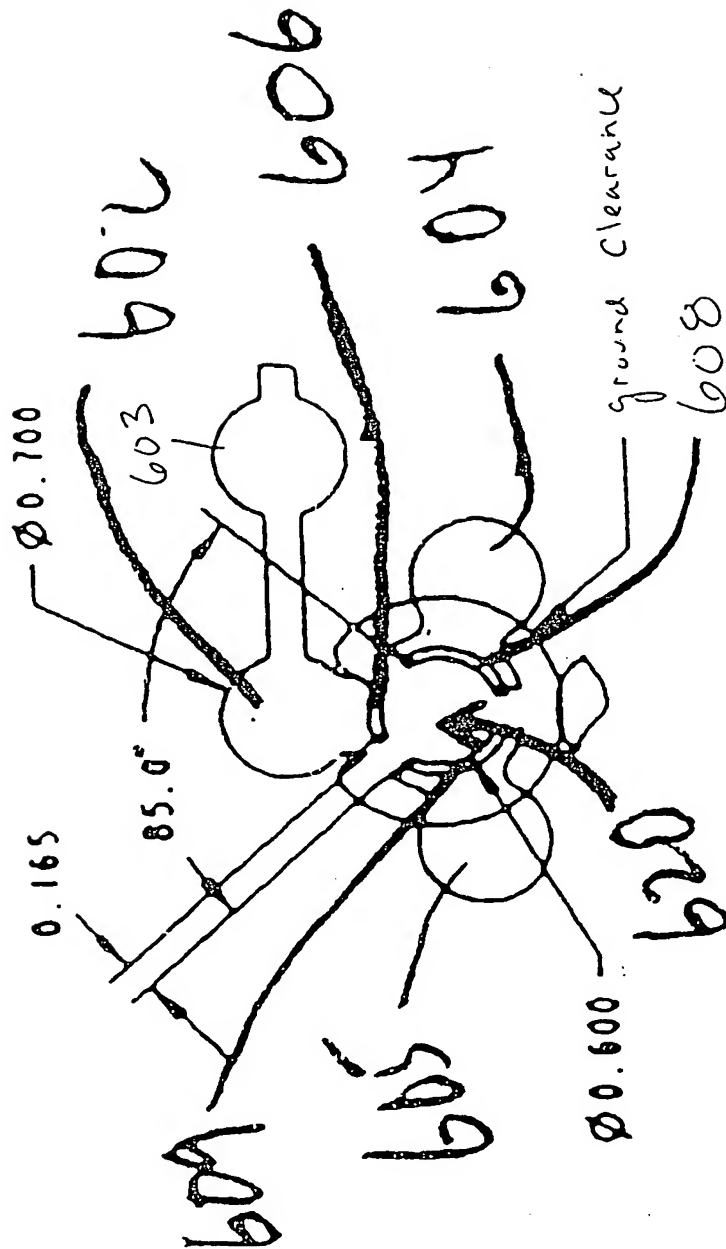


FIG 22A

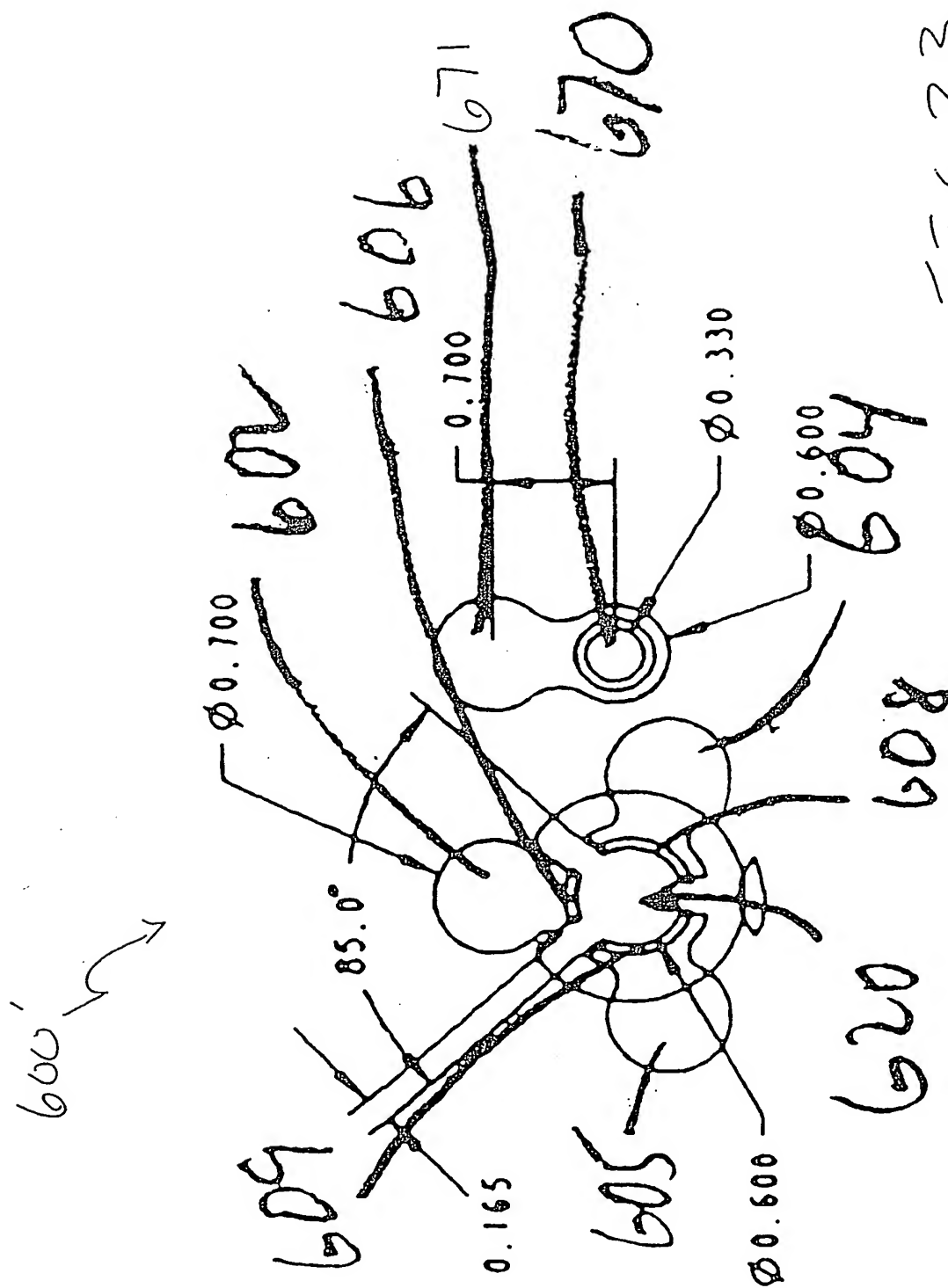


FIG. 23

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CORRECTED VERSION

(19) World Intellectual Property Organization
International Bureau(43) International Publication Date
21 December 2000 (21.12.2000)

PCT

(10) International Publication Number
WO 00/78105 A1(51) International Patent Classification?: **H05K 1/11**(74) Agent: **DROZENSKI, Diane, C.;** Teradyne, Inc., 321 Harrison Avenue, Boston, MA 02118 (US).(21) International Application Number: **PCT/US00/15551**(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.(22) International Filing Date: **5 June 2000 (05.06.2000)**(25) Filing Language: **English**(26) Publication Language: **English**

(30) Priority Data:

60/138,730	11 June 1999 (11.06.1999)	US
60/139,063	11 June 1999 (11.06.1999)	US
60/143,320	12 July 1999 (12.07.1999)	US
09/360,002	23 July 1999 (23.07.1999)	US

(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW). Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM). European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).(71) Applicant: **TERADYNE, INC.** [US/US]; 321 Harrison Avenue, Boston, MA 02118 (US).

Published:

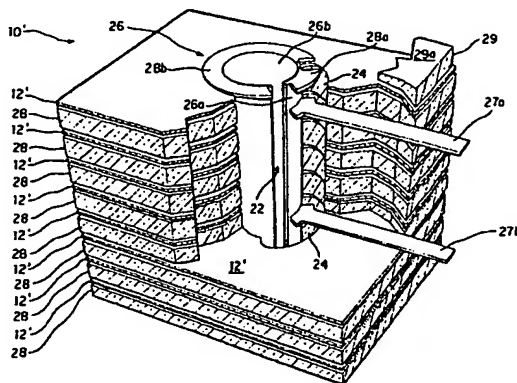
— with international search report

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(48) Date of publication of this corrected version:

13 June 2002

[Continued on next page]

(54) Title: **MULTI-CONNECTION VIA**

WO 00/78105 A1

(57) Abstract: An interconnection circuit and related techniques are described. The interconnection circuit (10) includes a plated through hole (26) having a plurality of electrically isolated segments (26a, 26b) with at least one of the plurality of electrically isolated segments (26a) coupled to a signal path (27a, 27b) and at least one of the electrically isolated segments (26b) coupled to the ground (12). With this arrangement, the circuit provides a signal path between a first and a second different layers of a multilayer. By providing one segment (26a) as a signal segment and another segment (26b) as a ground segment the size and shape of the electrically isolated segments (26a, 26b) can be selected to provide the interconnection circuit having a predetermined impedance characteristic. The interconnection circuit can thus be impedance matched to circuit board circuits, devices and transmission lines, such as striplines, microstrips and co-planar waveguides. This results in an interconnection circuit which maintains the integrity of relatively high-frequency signals propagating through the interconnection circuit from the first layer to the second layer. The interconnect circuits can be formed by creating distinct conductor paths (26a, 26b) within the cylindrical plated through-holes (26) using variety of manufacturing techniques including, but not limited to, broaching techniques, electrostatic discharge milling (EDM) techniques and laser etching techniques.



(15) Information about Correction:

see PCT Gazette No. 24/2002 of 13 June 2002, Section II

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

MULTI-CONNECTION VIA

5

GOVERNMENT RIGHTS

Not applicable.

RELATED APPLICATIONS

10 This application claims priority under 35 U.S.C. §119(e) from Application Nos. 60/138,730 and 60/139,063 each filed June 11, 1999 and Application No. _____, filed July 12, 1999 entitled Multi-Connection Via and Related Circuits and Techniques having named inventor Sepehr Kiani all of which are hereby incorporated herein by reference in their entirety.

15

FIELD OF THE INVENTION

This invention relates generally to electrical connections between layers of multi-layer printed circuit boards and more particularly to a class of layer-to-layer interconnections referred to as via circuits or more simply vias.

20

BACKGROUND OF THE INVENTION

As is known in the art, there exists a class of electrical connection structures, referred to as plated through holes (PTHs) or via circuits or more simply vias, which provide layer-to-layer interconnections in multi-layer printed circuit boards (PCBs).

25

A conventional via in a multi-layer PCB is typically provided by drilling or otherwise forming a hole through the PCB. The through hole passes through all conductive layer traces in the PCB which are intended to be connected. The hole is then plated to form an electrical connection among the conductive traces. In this manner, electrical connections between layers of multi-layer PCBs can be provided.

30

This process can be used to provide a signal path through which a single signal propagates between layers of a PCB. Connections to conductive traces or signal paths in each of the PCB layers can be made. This via connection technique conserves space on the PCB and thus allows PCBs to be more densely populated.

5

The via has been the mainstay of layer-to-layer interconnection since the inception of double-sided and multi-layer boards. Originally vias served dual purposes, providing layer-to-layer interconnect and through-hole component mount. The growth of surface mount component technology (with the exception of backplane connectors and other large devices), however, has reduced the need to utilize vias for through-hole component mount and has resulted in the via primarily providing layer-to-layer interconnection.

There has, however, been a trend to provide PCBs having increasingly higher circuit density and higher circuit speed. To help meet the demand for increased circuit density, it has been proposed to provide more than one independent signal path or connection in a single via. To provide multiple connections in the same via of a PCB, the via is formed as described above. Discrete connections are then formed among the conductive traces of the PCB by establishing grooves in the plating of the via to electrically isolate segments of the PCB. This technique permits two or more independent connections to be made in the same via of a multi-layer PCB. This technique further conserves space on the PCB and thus allows PCBs to be even more densely populated

Despite the advances made in increasing circuit density on PCBs, the high performance requirements of modern integrated circuit (IC) devices impose requirements for increasingly higher density of interconnections on PCBs so that the PCBs can accept the large number of input and output signal lines from IC devices which are packaged into increasingly smaller volumes. All of these design and

performance considerations add to the difficulties in attempting to lower PCB production costs which are increasing due to the use of complicated multiple-layer substrates.

5 Furthermore, modern IC devices operates at increasingly higher frequencies. As clock frequencies of circuits used on PCBs exceed 100 MHz, the electrical characteristics of PCB traces resemble high-speed signal transmission lines rather than D.C. electrical circuits. The higher clock frequencies and resultant shorter signal rise times expose PCB performance limitations which are manifested by signal integrity
10 phenomena such as ringing, reflections, ground bounce, and crosstalk.

 State of the art computer motherboards operate at frequencies of 100MHz and above, while telecommunications and high performance systems use device to board frequencies an order of magnitude higher. High performance systems having chip-to-
15 board clock speeds in the GHz range are expected. To support these current and future performance demands, improvement gains in PCB technology are required.

 To address the above density and speed concerns "buildup technologies" such as photo-via redistribution, and sheet buildup, have been developed. These techniques
20 have increased PCB performance significantly. These techniques, however, rely on thinner layers and use chemical etching (photo-defined vias), laser ablation, or plasma etching technologies to drill holes and connect PC board layers. Thus, such techniques are not appropriate for use in PCBs which include a relatively large number of layers between signal paths which must be connected.

25 So-called micro-vias have also been proposed. Both the signal and density performance of micro-vias are very good in comparison to drilled vias. There are still discontinuities in the signal path, because the ground plane is disrupted. However, because the scale is so small, this problem is minimal, especially when only going

through one layer (which does not break the continuous ground path). Micro-vias are particularly useful in applications in which the number of PCB layers is relatively small or where density is extreme, such as in micro ball grid array (μ BGA) escapement. As an added benefit, micro-vias can be placed directly in a surface
5 mount pad.

Because micro-vias must be manufactured from the outer surface (often out of non-woven aramid reinforced layers or unreinforced dielectric), the micro-vias can only be on the outer traces unless subsequent layers are built on top of the constructed
10 panel. Each layer adds significant processing cost. Via depth is limited greatly because the plating chemistry cannot flow through small blind holes in the same manner as through-hole vias. Similar limitations exist for laser ablated and co-deposition vias. Thus, micro-vias are also not particularly useful in PCBs which include a relatively large number of layers between signal paths which must be
15 connected.

Furthermore, none of the above techniques address the problem of maintaining signal strength and quality (i.e. shape of signal, lack of noise from either internal reflections or cross talk from other lines) collectively referred to herein as signal
20 integrity as device operating frequencies increase and/or clock rise times decrease. Moreover, owing to the addition of noise as well as reflections due to impedance mismatches, signal quality suffers when the impedance of the layer-to-layer interconnection transmission structure changes, resulting in parasitic wave reflections and in some cases resonance. This results in a signal path having a relatively high
25 insertion loss characteristic. A secondary related effect is crosstalk, which relates to the electro-magnetic interference (EMI) between circuit structures. Thus, one problem with the prior art approaches is that they merely attempt to increase density on a printed circuit board and they fail to provide any mechanisms for maintaining signal integrity and signal quality.

It would, therefore, be desirable to provide an interconnection structure which provides a layer-to-layer signal path which is relatively low loss, which does not degrade signal performance, which maintains signal integrity and which allows increased density of connections. It would also be desirable to provide an interconnection structure which is easily adapted to work with existing PCB manufacturing techniques, components and the like.

It would further be desirable to provide an interconnection structure which reduces the number and magnitude of impedance discontinuities due to transmission structure changes and which reduces the amount of crosstalk between circuit structures.

SUMMARY OF THE INVENTION

It has, in accordance with the present invention, been recognized that although signal lines within a single printed circuit board (PCB) layer are provided having predetermined impedance characteristics (i.e. the impedance of the signal line is controlled), such impedance control is not available for conventional plated-through holes (PTHs) which are used to provide signal paths between different layers of the PCB. This lack of control of the impedance characteristics of the via results in relatively large impedance mismatches between the via and other circuits/circuitry. Thus, the vias have relatively high insertion loss characteristics due primarily to impedance mismatch.

Because the via are lossy, there has been a desire and need to minimize number of vias on PCBs. In an effort to minimize the number of vias, circuit traces are ideally limited to a single plane (i.e. a single layer) in the PCB. Limiting the

circuit traces to a single plane, however also limits the number of possible circuit layout which are available to a circuit board designer.

5 In accordance with the present invention, an interconnection structure for providing a signal path between a first layer and a second different layer of a multi-layer structure includes a via having a plurality of electrically isolated segments with at least one of the electrically isolated segments coupled to a signal path and at least one of the electrically isolated segments coupled to ground. With this particular arrangement, a multi-connection via (MCV) which does not degrade signal
10 performance, signal integrity or signal quality of relatively high frequency signals is provided. By coupling a first segment of the via to a signal path and having a second segment of the via in proximity to the first segment coupled to ground, a defined electric field pattern is established in the via when signals having a relatively high frequency propagate through the via. By providing a structure through which a signal
15 can propagate with a defined electric field pattern, the MCV provides a signal path having a relatively low insertion loss characteristic to relatively high frequency signals propagating therethrough. The impedance characteristic of the via can be selected by appropriately selecting a variety of via characteristics including but not limited to the hole diameter of the via and the relative widths of the signal and ground segments.

20

This allows manufacture of printed circuit boards (PCBs) which include vias having a relatively low insertion loss characteristic and a relatively low return loss characteristic. The vias provide signal paths having a relatively low insertion loss characteristic because the vias can be designed and manufactured having defined
25 impedance characteristics. The via can thus be designed to better match (in an impedance matching sense) the IC devices or circuits or signal paths coupled thereto. Because the via of the present invention provides a relatively low loss, reliable signal path between layers of a multi-layer printed circuit board, it is not necessary to restrict

the PCB circuit layouts to a single layer or plane. Consequently reducing the number of required layers in a PCB.

Furthermore the MCV of the present invention can be provided having
5 multiple signal segments and/or multiple ground segments to thus allow inclusion of more signal traces in a single via. This allows the manufacture of PCBs having relatively high circuit density. The MCV of the present invention allows impedance control of signal paths between layers of a multi-layer PCB and thereby allows use of a connector which integrates tightly with the PCB. This type of impedance control is
10 not possible with conventional via technologies, including advanced structures such as micro vias. Thus the MCV of the present invention. This ability fundamentally changes routing rules for high speed signal traces, allowing for layer changes without concern of signal degradation. Furthermore, signal performance of the co-cylindrical wave-guide structure is completely independent of diameter. Moreover, MCVs
15 having multiple signal and ground segments which provide improved electrical performance allow further increases in connection density.

The MCV may be considered as a "shielded via" which offers improved performance to connectors and devices without requiring design changes of the PCB.
20 connectors or devices. That is, the MCV of the present invention is compatible with conventional PCB manufacturing processes including PCB via manufacturing processes.

To construct multi-connection vias in PCBs for signal experiments, a broach
25 process can be used to segment plated-through holes to provide isolated segments. Alternatively, MCVs can be provided using an electrical discharge machining (EDM) process. In utilizing the EDM process it should be noted that to properly utilize an EDM process to manufacture the multi-connection vias, it is necessary to provide a signal path from each of the individual segments of the via to ground during the EDM

process.

In accordance with a still further aspect of the present invention a method of routing signal traces in multi-layer printed circuit board using a multi-connection via (MCV) includes the steps of providing a multi-connection via having at least a pair of
5 signal segments and at least one ground segment, connecting a first signal trace to a first one of the pair of signal segments, connecting a second signal trace to a second different one of the pair of signal segments and connecting the ground segment to a groundplane layer of the multi-layer printed circuit board. With this arrangement, a
10 technique for reducing the number of vias provided in a multi-layer printed circuit board to route signal traces between different layers of the multi-layer printed circuit board is provided. This routing technique utilizing MCVs finds particular applicability when routing high speed signal traces in PCBs and maintaining signal integrity is an important concern.

15

In accordance with a still further aspect of the present invention, a multi-connection via launch includes a connector having a signal contact and ground contact disposed in an MCV. The MCV includes a ground via segment coupled to a ground plane and the ground contact of the connector and a signal via segment coupled to a
20 signal trace and the signal contact of the connector. Since the impedance characteristics of the MCV can be controlled, the MCV can act as an impedance matching structure between the connector and the signal trace on the PCB. This arrangement solves the problem of device and connector launch to the PCB which represents a major discontinuity in a signal path. The performance benefits provided
25 by the MCV's impedance-controlled structure throughout the transition thus carry over to PCB connector and device launches.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing features of the invention, as well as the invention itself may be more fully understood from the following detailed description of the drawings, in which:

5 FIG. 1 is a perspective diagrammatical view of a multi-connection via;

FIG. 1A is a perspective diagrammatical view of a multi-connection via;

FIG. 1B is a top view of a symmetrically split multi-connection via;

10

FIG. 1C is a top view of a non-symmetrically split multi-connection via;

FIG. 1D is a diagrammatical perspective view of a multi-connection via launch;

15

FIGs. 2 – 2C are a series of top views illustrating different single-ended via structures;

20 FIGs. 3 – 3E are a series of top views illustrating different examples of differential via structures;

FIGs. 4-4B are a series of views illustrating clusters of multi-connection vias;

FIG. 5 is a diagrammatical illustration of a parallel split pads;

25

FIG. 6 is a diagrammatical illustration of a radial split pads;

FIGs. 7A – 7C are a series of views illustrating a pad stack prior to drilling and plating steps;

FIGs. 8A – 8C are a series of views illustrating a pad stack after drilling and plating steps;

5 FIG. 9 is a perspective view of a two-dimensional split via;

FIGs. 10 and 10A are a series of diagrammatical perspective views of in via signal traces;

10 FIG. 11 is a perspective view of a buried multi-connection via;

FIGs. 12-12E are a series of plan views illustrating signal trace routing paths through vias;

15 FIG. 13 is a perspective view of a connector having a plurality of contact pairs press fit into a multi-connection via;

FIG. 13A is a cross-sectional view of a differential connection in a multi-connection via;

20

FIG. 13B is a cross-sectional view of a single-ended connection in a multi-connection via;

FIG. 13C is a perspective view of a connector having a triplet contacts press fit
25 into a multi-connection via;

FIG. 13D is a cross-sectional view of a differential connection in a multi-connection via;

FIG. 14 is a perspective view of a connector having a pair of signal contacts and a pair of ground contacts press fit into a multi-connection via;

FIG. 14A is a cross-sectional view of the connector of FIG. 14 after insertion
5 into the multi-connection via;

FIG. 15 is a perspective view of a connector having an eye of the needle connector disposed above a multi-connection via;

FIG. 15A is a cross-sectional view of the connector of FIG. 15 after insertion
10 into the multi-connection via;

FIG. 16 is a cross-sectional view of a single-ended co-cylindrical waveguide;

FIG. 17 is a cross-sectional view of a differential co-cylindrical
15 waveguide;

FIGs. 18 and 18A are a series of perspective views which show a surface mount device disposed over and on, respectively, a multi-connection via;
20

FIGs. 19 and 19A are a series of perspective views which show a surface mount device having an eye of the needle connector disposed over and on, respectively, a multi-connection via;

FIG. 20 is a perspective view of a surface mount capacitor disposed over a multi-connection via;
25

FIG. 21 is a perspective view of surface mount connector coupled to surface mount pads of multi-connection vias provided in a multi-layer printed circuit board;

FIG. 21A is a top view of a multi-connection via provided in the second printed circuit board shown in FIG. 21;

5 FIG. 22 is a perspective view of a first printed circuit board having surface mount connectors coupled to multi-connection vias on a second printed circuit board;

FIG. 22A is a top view of a multi-connection via provided in the second printed circuit board shown in FIG. 21; and

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FIG. 23 is a top view of a multi-connection via provided in a printed circuit board.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

15 Before proceeding with a description of the figures, it should be noted that reference is sometimes made herein to multi-connection vias (MCVs) manufactured in a printed circuit board or multi-layer structure made from a particular material such as FR4. Those of ordinary skill in the art should appreciate that other materials suitable for manufacture of printed circuit boards and multi-layer structures may also be used.

20 Reference is also sometimes made herein to MCVs having a particular cross sectional diameter. It should be understood that MCVs having any diameter may be used. Also, MCVs having a substantially round cross-sectional shape are herein described. It should be appreciated that MCVs having other shapes including but not limited to oval, rectangular, square, triangular and irregularly shapes may also be used.

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Referring now to FIG. 1, a multi-layer printed circuit board (PCB) 10 (also sometimes referred to herein as a multi-layer structure 10) includes a plurality of layers 12a-12h, generally denoted 12 each of which corresponds to a ground plane layer. Each of the ground plane layers 12 may be provided from a conductive material

(e.g. a sheet of copper foil) which is typically supported by a support structure such as a dielectric core material, for example. The ground plane layers 12 may be disposed, deposited, attached or otherwise provided on the support structures using any well-known technique. PCB 10 also includes a plurality of signal traces 14a – 14c, generally denoted 14 which are disposed on different signal layers of the PCB 10. It should be noted that in FIG. 1, to promote clarity in the figure, the dielectric cores or other structures which support each of the ground plane layers 12 and the signal traces 14 are not shown. By way of terminology, the layers of PCB 10 on which signal traces (such as signal traces 14a – 14c) are disposed are referred to as signal trace layers or more simply signal layers. Similarly, the layers of PCB 10 on which are disposed ground planes (such as ground planes 12) are sometimes referred to as ground planes or more simply ground layers. Similarly again, the layers of PCB 10 on which power signals are disposed are sometimes referred to as power layers or power planes.

Although the signal traces 14a, 14c are disposed on different layers of the multi-layer structure 10, they are electrically coupled through an interconnection device 16. Interconnection device 16 is a multi-connection via (MCV) 16 which can provide multiple signal paths between any of the signal traces 14 on any signal layer of the multi-layer structure 10. MCV 16 is provided from conductive material disposed on the walls of an opening in the multi-layer structure. The conductive material is disposed to form a plurality of separate segments 18a, 18b, 20a, 20b which are electrically isolated from each other. Although MCV 16 is here shown having four electrically isolated segments 18a, 18b, 20a, 20b, it should be appreciated that MCV 16 can be provided having fewer or greater than four segments. The particular number of segments to be provided in an MCV depends upon a variety of factors including, but not limited to, the particular application, the number of signal traces to be connected and the limits on mechanical tolerances and printed circuit board processes imposed by manufacturing techniques.

In one embodiment, the opening in the multi-layered structure 10 is provided as a conventional plated through hole (PTH) which is then "split" to provide the electrically isolated segments. It should be noted that portions of the layers 12 and interconnection device 16 have here been removed to promote clarity in the figure. Thus, a portion of segment 20b is shown in phantom and in this particular embodiment, segment 20b has a size, shape and function similar to segment 20a. Segments 18a, 18b have pad regions 19 (or more simply pads 19) while segments 20a, 20b have pads 21a – 21d generally denoted 21. The purpose of the pads 19, 21 will be described below.

In this particular embodiment, segments 18a, 18b, 20a, 20b are electrically isolated from each other by providing spaces or splits generally denoted 22 between each of the segment 18a, 18b, 20a, 20b, in the MCV 16. In this example, split 22a is between segments 18b and 20a, split 22b is between segments 20a and 18a, split 22c (only partially visible in FIG. 1) is between segments 18a and 20b and split 22d (not visible in FIG. 1) is between segments 20b and 18b. It should be noted that a variety of different manufacturing techniques can be used to electrically isolate the segments 18a, 18b, 20a, 20b. Thus, the term "split" should not be misconstrued to imply that the only technique to provide the electrically isolated segments 18a, 18b, 20a, 20b is mechanical cutting or splitting of the conductive material which forms the walls of the hole in the multi-layer structure 10.

It should also be noted that a variety of different techniques for manufacturing the isolated segments 18a, 18b, 20a, 20b, including, but not limited to, abrasive waterjet cutting, broaching, laser machining, milling, EDM, ultrasonic machining, selective patterning or deposition, selective plating and chemical etching processes can be used. Also, so-called non plating processes involving the use of conductive inks applied by either printing or screening processes can also be used.

It should further be noted that the operation and advantages of the MCV 16 as well as other MCV structures described herein are independent of the particular manufacturing techniques used to provide the MCVs. Any manufacturing technique including but not limited to those mentioned above, which can reliably be used to manufacture high quality, reliable MCVs and PCBs may be used. The particular manufacturing technique which is used in any application will depend on a variety of factors including but not limited to the purpose of the particular application (e.g. space, military, commercial), the cost of the manufacturing process (including development costs as well as the costs of start-up tooling or machinery) compatibility with standard PCB manufacturing processes, the quality with which the MCVs and PCBs can be manufactured compared with the quality of the MCVs and PCBs required for the application, production rate required for a particular application, circuit geometry generation capabilities vs. circuit geometry required in any particular application and control and scale of feature parameters of the MCV and PCB.

Since the segments 18a, 18b, 20a, 20b are electrically isolated, the segments may be independently coupled to different circuit structures or components (e.g. signal or ground paths, IC devices, etc...) of the multilayer structure 10. As shown in FIG. 1, segments 18a, 18b are each coupled to ground plane 12a via pads 19. Thus, segments 18a, 18b are effectively coupled through the ground plane 12a on PCB 12a. Similarly, segments 20a, 20b are coupled to respective ones of the signal paths 14a, 14b through pads 21b, 21c.

Pad 21a is disposed on a top layer dielectric layer of PCB 10 and pad 21d is disposed on a bottom dielectric layer of the PCB 10. Pads 21a, 21d are not coupled to signal traces. It should be noted that in some applications it may be desirable to provide pads 21a, 21d having a size and shape which is different that the size and shape of pads 21b, 21c. As will be described further below in conjunction with FIG.

1C and FIGs. 7-8C, the widths W_s of pads 21a-21d are selected to both accommodate mechanical tolerances in the manufacture of MCVs and to help provide a good impedance match to the respective signal path or circuit component coupled thereto.

5 It should be appreciated that portions 24a, 24b of each of the ground plane layers 12 of PCB 10 are removed over the regions where the signal segments 20a, 20b of the MCV exist to help reduce impedance discontinuities and control impedance values in the signal segments 20a, 20b.

10 As mentioned above, signal paths 14a and 14c are on layers of different ones of the PCBs 12. Each of the signal traces 14a, 14c have a first end coupled to respective ones of pads 21b, 21c which in turn are coupled to signal segment 20a. Thus, signal segment 20a provides an electrically conductive signal path between signal traces 14a and 14c.

15 The impedance characteristics of segment 20a presented to signal paths 14a, 14b can be controlled by selection of the dimensions of the MCV structure 16. In particular, by selecting the relative shapes and dimensions of the signal segments and ground segments as well as the shapes and dimensions in the openings in the ground
20 plane layers (e.g. portions 24a, 24b) the MCV can be provided having signal path performance characteristics required for supporting the signal bandwidth of current and future devices used in multi-layer structures such as multi-layer structure 10. As is known, there is a trend to use devices which operate at increasingly high clock
25 frequencies. As high frequency signals propagate along signal traces of PCBs, the integrity of the signals as they traverse between different layers of a multi-layer structure must be preserved. The impedance-controlled MCV structures 16 of the present invention provide appropriate vehicles for such transmission.

If a signal path is perfectly impedance matched, the signal will experience no

impedance transitions which provide points of energy loss. The only losses in a perfectly impedance matched signal path are those from the dielectric (i.e. attenuation), which are length-of-trace dependent. Attenuation is a significant problem in relatively large PCBs, such as backplanes, where the trace lengths of the signal paths are long compared to the wavelength of the signal. When there are impedance discontinuities in the signal path, additional energy is lost and the signal propagating along the path is weakened. This lost energy has several effects on the circuit.

First, part of the signal is reflected back towards the source. This reflection can manifest itself as noise on the signal path. If two impedance mismatches are spaced by a distance approximately an integer multiple of a quarter-wavelength of the signal frequency, the reflections will resonate between the impedance mismatches. A common case is that of short unterminated lines (also sometimes referred to as stubs), where the signal propagates to the end of a signal trace that is terminated in either an open or a short circuit (i.e. the end of the signal trace is not connected to any structure intended to provide an impedance matching function) thereby causing all of the signal energy to be reflected.

Second, if the signal path is not fully controlled (e.g., completely bound by ground structures) within the range of other signal carrying lines, electromagnetic interference (EMI) will result. EMI reduces the energy of the signal, and these free energy waves cause or induce crosstalk to other circuits. Crosstalk refers to the inducement or coupling of a signal from one signal trace or line to another signal trace or line. A crosstalk signal is a signal which is induced on one signal line from the electromagnetic field surrounding a signal line on which a signal is propagating. A crosstalk signal can occur from between a board and a device above the board and manifest itself as noise on signal lines physically proximate to the signal line on which a signal was originally propagating. Devices typically have maximum noise levels

having equal arc lengths L_s , L_g respectively. Regions 29a, 29b may be provided as dielectric regions (e.g. provided from portions of a PCB in which the MCV 26' is formed) or from air filled spaces.

5 In one particular example, a symmetrically split MCV 26 was provided having a diameter of about 0.559 mm and the width of gap regions 29a, 29b was varied. When the gap increased, the signal conductor and ground conductor arc lengths were decreased by an equal amount to thus maintain symmetry. The closest coupling
10 W_{gap} of the gap 29a, 29b has a significant effect on such coupling and therefore on reflection and transmission characteristics of the MCV. The best results were achieved with a gap width of about 254 μm .

15 Examination of test results reveals that the reflections drop off to near zero as the gaps 29a, 29b were widened until a gap width was reached at which the reflection was a minimum. It is expected, however, that if the gaps were widened beyond a certain point, (requiring a larger diameter MCV) the reflected power would eventually increase.

20 The energy that is reflected in a conventional PTH increases at a greater rate than that of MCVs with frequency. Thus the benefits of the MCV structure is greater at higher frequencies. In a best-tuned case, the reflected energy by the MCV is negligible across the frequency range. The stubs formed by those portions of the multi-connection via segments which extend above and below the signal traces
25 coupled to the via segments can dominate reflection characteristics of the MCV. Relatively large reflections can occur at frequencies corresponding to resonant frequencies of the stubs. In some cases pads (e.g. pads 21a, 21d in FIG. 1) at the end of the MCV may also be a source of reflections..

Examination of experimental test results show that transmission is consistent with the reflections. A decrease in reflected power increases the transmitted power proportionally. This is an important interaction to note, since it is possible to decrease both the reflection and the transmission, e.g. if losses due to EMI are high.

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Examination of experimental results to determine the affect of varying the conductor ratio on reflections and transmissions shows that varying the arc length L_s of the signal conductor 26a tunes the MCV structure somewhat better than varying the width W_{gap} of the gaps 29a, 29b and keeping the arc lengths L_s , L_g of the ground and signal segments 26a, 26b symmetric. In this case, as the signal arc-length decreases below 520 μm , the reflections begin to increase at higher frequencies. This implies that these via structures are inherently tunable to the circuit to which the MCV is coupled (e.g. transmission lines 27a, 27b in FIG. 1A). Conventional PTHs can attain some performance gains by decreasing the size and increasing the ground clearance, (both of which are difficult to achieve) but otherwise provide no means for true impedance tuning.

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Examination of experimental test results to determine the affects of varying the diameter of MCVs on reflections and transmissions reveals that reducing the signal arc length L_s reduces reflections to the same range as MCVs having smaller diameters. Thus, an MCV having a relatively large cross-sectional diameter is as tunable as an MCV having a relatively small cross-sectional diameter. This is in contrast to conventional PTH approaches in which increasing the via diameter increases the reflections and decreases the transmission, thus indicating sensitivity to diameter.

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The above tuning characteristic of MCVs is significant in that it indicates that larger diameter MCVs, which are easier to manufacture, employ better impedance control than the smallest conventional PTH. In other words, reflections and transmission in conventional PTHs are highly sensitive to cross-sectional diameter, while impedance-tuned MCVs are not.

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Referring now to FIG. 1D, a connector 30 having a signal contact 32 and ground contact 34 partially disposed in an MCV 36 provides a multi-connection via launch (an MCV launch). The MCV 36 is provided in a portion of a printed circuit board (PCB) 37 which may be provided from a dielectric material such as FR4 or any other material having similar mechanical and electrical characteristics or otherwise suitable for manufacture of PCBs. The MCV 36 includes a ground via segment 38 coupled to a ground plane 39 and a signal via segment 40 having a signal trace 42 coupled thereto.

In one particular example, the MCV launch is provided having a diameter of about 1.5 mm since at this diameter the MCV launch is easily manufactured and provides space for a pair of contacts. The arc length of the signal via segment 40 is selected to be about 540 μm and the gap or split 43 between the ground via segment 38 and the signal via segment 40 is about 254 μm . A signal is launched into the PCB signal trace 42 and exits on a connector (the launch portion of which is shown in FIG. 1D) both of which are impedance matched to 50 Ω . With these parameters, a relatively good impedance match is provided between the connector and the PCB signal trace 42.

Since the impedance characteristics of the MCV 36 can be controlled, the MCV 36 can act as an impedance matching structure between the connector and the signal trace 42 on the PCB. This arrangement solves the problem of device and connector launch to the PCB which represents a major discontinuity in a signal path. The performance benefits provided by the MCV's impedance-controlled structure throughout the transition thus carry over to PCB connector and device launches.

Referring now to FIGS. 2 – 2C a series of views illustrating single end via structures are shown. In FIGS. 2-2C, like reference designations correspond to like

elements throughout the several views. As shown in FIG. 2, an MCV 44 includes a signal line segment 45 and a ground segment 46 which are electrically isolated from each other. It should be noted that in this particular embodiment, the signal and ground segments 45, 46 are provided having equal arc lengths (also sometimes referred to herein as "widths"). The signal and ground segments 45, 46 are provided by forming a hole in a PCB and depositing, plating or otherwise providing conductive material on the surface of the PCB which defines the hole. The signal and ground segments 45, 46 are electrically isolated by forming non-conductive regions 48. Regions 48 represent printed circuit board areas exposed during drilling and/or other procedures performed to provide the MCV 44 and the nonconductive spaces 52 between the signal line segments 45 and the ground segment 46. To prevent exposed PCB regions 48 (and in particular surface 52) from absorbing moisture and to otherwise protect the regions 48 (and in some cases to strengthen the MCV 44), a central region 50 of the MCV 44 is filled with a material which may, for example be provided as a dielectric material such as an epoxy. It should be noted that in some applications, sealing may not be required..

A ground plane 53 is disposed about MCV 44 and electrically contacts the ground segment 46. Regions of the ground plane 53 have been removed to provide nonconductive areas 54. As explained above in conjunction with FIG. 1, in preferred embodiments, no conductive material is present in the region of a signal line 56 contacting the signal line segment 45 and thus the ground plane 53 is provided having a non-symmetric pattern in the region of the MCV:

The width of the gaps 52, the arc lengths of the signal and ground segments 45, 46, the diameter of the hole 48 and the layer combinations (e.g. thickness, relative dielectric constant, number of layers, etc...) of the PCB may all be varied to provide the MCV 44 having a predetermined impedance characteristic.

Referring now to FIG. 2A, it should be noted that the signal and ground segments 45, 46 are provided having un-equal arc lengths. In this particular embodiment, the arc length of signal segment 45 is smaller than the arc length of ground segment 46. In other embodiments, however, it may be desirable to provide signal segment 45 with an arc length which is greater than the arc length of ground segment 46. In this case, other features (e.g. spacing between the ground and signal segments, 45, 46, diameter of the MCV, etc. can be selected to provide an MCV having an appropriate impedance characteristic.

The MCV embodiments of FIGs. 2 and 2A were tested by providing layer connections between like spaced layers signal layers. The signal arc length was varied but the diameters of the MCVs were kept the same in all tests.

The results of the tests are summarized in Table I below which shows the reflection amplitude for a variety of different signal conductor arc lengths for MCVs having a diameter of 1.5mm.

Table I

Signal conductor arc length	Reflection amplitude
0.19mm	2.0%
0.31mm	1.0%
0.49mm	2.2%
0.74mm	3.6%
0.90mm	3.0%
1.09mm	8.4%
2.13mm	12.7%

Examination of Table I reveals that an MCV having a relatively large diameter with a wide signal conductor arc length has worse performance than a via having a smaller diameter. As the arc length is decreased, the reflection reduces to near zero

(in the case where L_s equals 0.31mm) and then the reflection increases again (in the case where L_s equals 0.19mm). It is interesting to note that in digital electronics, vias are capacitive in nature (i.e., yielded negative broadband reflection), while the over compensated multi-connection via here is inductive.

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Referring now to FIG. 2B, an MCV 44 includes a pair of signal segments 45 and a pair of ground segments 46 symmetrically disposed about a central longitudinal axis 49 of the MCV 44. The signal and ground segments 45, 46 are each provided having equal arc lengths. It should be noted however, that in some applications it may not be desirable or necessary to provide the signal and ground segments having equal arc lengths. For example, the width of the signal segment may be selected to correspond to the width of a signal trace which terminates on the signal segment of the MCV.

15 Referring now to FIG. 2C, an MCV 44 includes triplet signal segments 45 and triplet ground segments 46 symmetrically disposed about a central longitudinal axis 49 of the MCV 44. The signal and ground segments 45, 46 are each provided having equal arc lengths.

20 Referring now to FIGs. 3 – 3E a series of views illustrating differential via structures are shown. The primary difference between a single-ended MCV and a differential MCV is that in a single-ended MCV the signal propagates between ground return structures. In the differential case, the return path is a discrete conductor equal and opposite to another conductor. The ground in a differential signal acts as a drain for leakage caused by symmetry imperfections. In PCBs which include circuit components operating at relatively high clock speed (i.e. high-frequency circuits) differential signal pairing may provide performance advantages, especially for long traces. In FIGs. 3-3E, like reference designations correspond to like elements throughout the several views.

As shown in FIG. 3, an MCV 60 includes signal line segments 61a, 61b which are provided by plating, depositing or otherwise adhering a conductive material to the walls of a hole formed in a PCB. The central portion 62 of MCV 60 is filled with a dielectric such as air or an epoxy. Portions 63 represent printed circuit board areas exposed during drilling and other procedures to provide the MCV 60 and the signal line segments 61a, 61b. It should be noted that in this particular embodiment, the signal line segments 61a, 61b are provided having equal arc lengths. In the case where the structure is for a differential signal the signal segments must be symmetric top achieve desired transmission and reflection characteristics.

A ground plane 64 is disposed about MCV 60. Although not shown in this view, it will be appreciated by one of ordinary skill in the art that multiple layers of the PCB in which the MCV exists may correspond to ground plane layers. This is also true of each of the embodiments of FIGs. 3-3E. Signal lines 58a, 58b and signal line segments 61a, 61b to which the signal lines 58a, 58b are respectively coupled are on different layers than the ground plane 64 and thus are electrically isolated from the ground plane 64. In FIG. 3, one differential signal pair (i.e. signal lines 58a, 58b) couples to MCV 60 on one signal layer and a second differential signal pair (not visible in FIG. 3) couples to MCV 60 on a second different signal layer. Portions of the ground plane 64 have been removed to provide nonconductive areas 65. It should be noted that signal lines 58a, 58b connect to MCV segments 61a, 61b toward a first end of the segments 61a, 61b. It should be noted that the traces coming into a differential via will also be of differential construction (e.g. differential stripline or microstrip construction). Thus, the signal traces will have a particular spacing which ideally will be maintained right up to the via.

The width of the gaps 63, the arc lengths of the signal segments 61a, 61b, the diameter of the hole 62, ground clearance distance and shape 65, and the layer

combinations (e.g. thickness, relative dielectric constant, number of layers, etc...) of the PCB may all be selected to provide MCV 60 having a predetermined impedance characteristic.

5 Referring now to FIG. 3A, it should be noted that in this embodiment, a ground segment 64a is disposed between two ends of the differential signal paths 61a, 61b. The signal and ground segments 61a, 61b and 64a are each provided having equal arc lengths.

10 The width of the gaps 63, the arc lengths of the signal segments 61a, 61b, and ground segments 64a, the diameter of the hole 62, ground clearance distance and shape 65, and the layer combinations (e.g. thickness, relative dielectric constant, number of layers, etc...) of the PCB may all be varied to impact the impedance characteristics of the MCV 60.

15 Referring now to FIG. 3B, it should be noted that in this embodiment, the ground segment 64a is disposed between two ends of the differential signal segments 61a, 61b. The signal segments 61a, 61b are each provided having equal arc lengths while the arc length of the ground segment 64a is smaller than the arc lengths of the
20 signal segments 61a, 61b. It should be noted that an equally effective alternative would be to provide the arc length of the ground segment 64a larger than the arc length of the signal segment.

As mentioned above in conjunction with FIG. 3A, the width of the gaps 63, the
25 arc lengths of the signal segments 61a, 61b, and ground segments 64a, the diameter of the hole 62, ground clearance distance and shape 65, and the layer combinations (e.g. thickness, relative dielectric constant, number of layers, etc...) of the PCB may all be varied to impact the impedance characteristics of the MCV 60.

Referring now to FIG. 3C, an MCV 60 includes signal line segments 61a – 61c which are provided in any suitable manner. In this particular embodiment, the signal line segments 61a – 61c are symmetrically disposed about a central longitudinal axis and are provided having equal arc lengths.

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The ground plane 64 is disposed about MCV 60 the signal lines 58a, 58b and signal line segments 61a – 61c to which the signal lines 58a – 58c are respectively coupled are on different layers than the ground plane 64 and thus are electrically isolated from the ground plane 64. Portions of the ground plane 64 have been removed to provide nonconductive areas 65. It should be noted that no drain is provided in this embodiment and that without a drain between multiple-differential pair sets, there is crosstalk. Thus, this embodiment would not be preferred.

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Referring now to FIG. 3D, an MCV 60 includes signal line segments 61a – 61f which are provided in any suitable manner. In this particular embodiment, the signal line segments 61a – 61f are symmetrically disposed about a central longitudinal axis and are provided having equal arc lengths. It should be noted that orientation of the signal line segments in each of FIGs. 3D and 3E can vary from hole to hole to provide the best trace routing in the PCB.

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The ground plane 64 is disposed about MCV 60 the signal lines 58a – 58f and signal line segments 61a – 61f to which the signal lines 58a – 58f are respectively coupled are on different layers than the ground plane 64 and thus are electrically isolated from the ground plane 64. Portions of the ground plane 64 have been removed to provide nonconductive areas 65. It should be noted that no drain is provided in this embodiment and that without a drain between multiple-differential pair sets, there is crosstalk. Thus, this embodiment would not be preferred.

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Referring now to FIG. 3E, an MCV 44 includes MCV signal line segments 61a – 61d a first ground segment 64a disposed between two the differential signal paths 61a, 61d and a second ground segment 64b disposed between two the differential signal paths 61b, 61c. The signal segments 61a – 61c are each provided having equal
5 first arc lengths and the ground segments 64a, 64b are each provided having equal second arc lengths. In some applications it may be desirable to make the first and second arc lengths equal lengths while in other embodiments it may be desirable to make the first and second arc lengths unequal(that is the differential pair signal segments should have equal arc lengths, but the ground drain can be provided having
10 and arc length which is either larger or smaller than the arc length of the signal segments.

In this particular embodiment, the ground segments 64a, 64b are diametrically opposed and the MCV signal line segments 61a – 61d are symmetrically disposed on
15 opposite sides of a plane of the MCV 60 which passes through ground segments 64a, 64b along a horizontal center line of the MCV 60.

The ground plane 64 is disposed about MCV 60 and the signal lines 58a – 58d and signal line segments 61a – 61d to which the signal lines 58a – 58d are respectively
20 coupled are on different layers than the ground plane 64 and thus are electrically isolated from the ground plane 64. Portions of the ground plane 64 have been removed to provide nonconductive areas 65. Ground segments 64a, 64b are coupled to ground plane 64. Because there is a ground drain between signal pairs experiments have show that there is no cross talk, therefore this configuration would be preferred
25 for multiple signal sets in a single via.

Referring now to FIGs. 4-4B in which like elements are provided having like reference designations throughout the several views, a series of clusters of multi-connection vias 66 are shown.

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Referring first to FIG. 4, a plurality of two-connection vias 66 clustered in pairs 67a, 67b define routing channels 68a, 68b which pass on either side of the clusters 67a, 67b. Ground vias 66a are juxtaposed with zero trace spacing between them. Because there is no need for a keep-out zone between the ground sides of the vias 66a, connection density increases.

Referring now to FIG. 4A, one electrical form of MCV that particularly benefits from multi-connection vias is the differential pair. In its simplest form, a differential pair MCV provides two connections over which can be transmitted signals in opposed phase. Because a perfectly balanced differential pair is not possible, it is desirable to have a ground drain close to the pair. FIG. 4A illustrates clusters 69a – 69d of three three-connection vias 60. Each three-connection includes a ground drain 70a and a differential pair (i.e. signal segments) 70b. The ground sides 70a of the MCVs 70 vias are juxtaposed in a zero trace condition and thus no keep-out zone is necessary thereby increasing connection density. The clusters 69a-69d are arranged to define routing channels 72a-72d which pass on either side of the clusters 69a-69d.

Referring now to FIG. 4B, a plurality of four-connection vias 76 are grouped in clusters 78a, 78b. Each four-connection via 76 includes a pair of ground drains 76a and a pair of signal segments 76b. The ground sides 76a of the MCVs 76 are juxtaposed in a repeating pattern which thus provides higher connection densities than prior art techniques. The clusters 78a, 78b are arranged to define a routing channel 80 which passes between the clusters 78a, 78b.

As demonstrated by the examples shown in FIGs. 4-4B, the possibilities for multi-connection via arrangements are numerous. One consideration in routing multi-connection vias is clearance around the via structure. The distance between the signal side (e.g. segments 76b) and the trace is much larger than that of the ground side (e.g. segments 76a), primarily due to the ground plane clearance. This clearance requires traces on the layers above and below the ground plane to not be routed in the

clearance areas, thereby avoiding potential impedance mismatch in the trace and minimizing crosstalk from the signal via. On the via ground side, the ground plane is uninterrupted, because there is little or no field on this side. Therefore, clearance on the ground side can be set to just outside a minimum annular ring requirement.

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It should be noted that the MCVs 66, 70 and 72 described above in conjunction with FIGs. 4-4B, may be provided having any of the appropriate geometries described above in conjunction with FIGs. 2 – 3E.

10 Referring now to FIG. 5, a multi-connector via 82 includes pad segments 82a-82f. The pad segments are each spaced by a gap 84. The gap edges 86 are parallel and thus provide so-called “parallel splits” between the pad segments 82a-82f.

The parallel split approach is in contrast to the so-called radial split approach
15 as illustrated in FIG. 6. In the radial split approach, a multi-connector via 88 includes pad segments 88a-88f. The pad segments 88a-88f are each spaced by a gap 84. The gap edges 89 are formed at an angle with respect to each other so that a straight line (here shown in phantom as lines 91) drawn along a plane defined by each edge 89 intersects a center point 90 which is located along a central longitudinal axis of the
20 MCV 88.

While MCVs with parallel and radial pad segments can be produced with equal ease, the parallel split provides greater arc length for traces to connect to. In some applications such additional arc length may be desirable since it may offer
25 additional flexibility, considering the difficulty in routing from a specific direction to the MCV.

Referring now to FIGs. 7 – 7C a series of views illustrating a pad stack prior to drilling and plating for a single conductor shielded via, where signal layers without connections have no pad.

5 Referring first to FIG. 7, a pattern to be etched or otherwise formed in top and bottom pad layers of a multilayer structure includes conductor regions 92 and 94 which will eventually correspond to a signal segment and a ground segment, respectively, of an MCV. Shown in phantom and indicated by reference numeral 95 is the diameter of hole to be drilled or otherwise provided (e.g. punched or cut) in a PCB
10 which will be plated to form the MVC.

As shown in FIG. 7A, a conductor region 96 having a radial shape is disposed on each layer of the multilayer structure which will include a signal trace to be coupled to the MVC. As shown in FIG. 7B, each layer of the multilayer structure
15 which will not include a signal trace does not include any conductor region in the area of the MVC. As shown in FIG. 7C a conductor region 97 provides a ground plane on the ground layers of the multilayer structure. Here portions 98 of the ground plane conductor 97 have been removed.

20 Once drilled, plated, and split, the pad stack appears as illustrated in FIGs. 8-8C. Referring first to FIG. 8, a hole 99 has been drilled through each of the layers. A portion of the conductor region 92 (FIG. 7) has been removed by the drilling process and the MCV signal segment 92' remains in the top and bottom pad layers as shown. Similarly, a portion of the conductor region 94 (FIG. 7) has been removed by the
25 drilling process and MCV ground segment 94' remains in the top and bottom pad layers. The plated through hole has been split to provide gaps 91 which define the signal and ground segments 92', 94'. As can be seen from FIGs. 8-8C, the splits 91 extend through each of the layers in the MCV.

As shown in FIG. 8A, a portion of the conductor region 96 (FIG. 7A) has been removed by the drilling process and an MCV signal segment 96' remains on each of the signal trace layers included in the multilayer structure. The signal segments 96' are each adapted to couple the MCV to a signal trace. As shown in FIG. 8B, each layer of the multilayer structure which will not include a signal trace still does not include any conductor region in the area of the MVC but does include a layer of conductive plating 93 disposed on the surface of the hole or "barrel" portion of the MCV. The plating material 93 is the conductor which electrically couples each of the layers through which the MCV passes. As shown in FIG. 8C the conductor region 97 provides a ground plane on the ground layers of the multilayer structure. The nonconductive region 98' is arranged above the signal segment pads 96' used to connect signal traces to the MCV.

Referring now to FIG. 9, a two-dimensional split via 100 including a multi-connection via 102 and a multi-connection via 104 are disposed within a multi-layer printed circuit board 110 as shown. The multi-connection via 102 includes a plurality of separate electrically isolated segments 106, each of which are connected to either a ground plane (not shown) or a signal trace (not shown) as required by the requisite circuitry of the printed circuit board 110 to connect circuitry (not shown) on one layer to another layer. The multi-connection via 104 includes a plurality of separate electrically isolated segments 108, each of which are connected to either a ground plane (not shown) or a signal trace (not shown) as required by the requisite circuitry of the printed circuit board 110 to connect circuitry (not shown) on one layer to another layer. The multi-connection via 102 and the multi-connection via 104 are disposed in the same hole within the printed circuit board 110, but electrically isolated from one another. A horizontal or radial split 105 exists between the two structures. In addition to increased layer-to-layer routing, horizontally-split vias can significantly reduce reflections caused by unused via extensions. In horizontal-split vias, each level operates as a separate set of connections, thereby improving space usage.

Referring now to FIGs. 10 and 10A, an alternative to splitting vias, is to create traces on the inside of a via cylindrical surface. It should be noted that in FIGs. 10 and 10A to promote clarity only conductive traces and segments are shown.

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As shown in FIG. 10, a signal trace 120 of one layer of a multi-layer printed circuit board can extend into a via 112 including a ground portion 116 and a signal portion 118 separated by a nonconductor 114 and connect to the signal portion 118. The signal portion 118 is also connected to a signal trace 122 on another layer of the multi-layer printed circuit board. With such an arrangement, a signal path from one layer can be connected to a signal path of another Layer and this arrangement also eliminates electrical stubs and EMI above and below the board from the via.

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As shown in FIG. 10A, a signal trace 120' of one layer of a multi-layer printed circuit board can extend into a via 112' including a ground portion 116 and a signal portion 118' and connect to the signal portion 118'. The signal traces 120', 122' approach MCV 112 from different angles on different layers of a multi-layer printed circuit board. The signal portion 118' of MCV 112 traverses in both horizontal and vertical directions (i.e. signal portion 120 "twists") to connect to a signal trace 120' to a signal trace 122'. With such an arrangement, a signal path from one PCB layer can be connected to a signal path extending at a different angle on another PCB layer. This technique can be used to provide flexibility in routing signal traces. For example, a signal trace must connect to a particular signal segment of an MCV and thus must be oriented in a particular manner relative the MCV. If the twist technique is used, then more options are available with respect to the orientation and location of MCV signal segments relative signal traces. The twist technique thus allows routing of signal traces to MCVs in the same manner that a signal trace would be routed to any plated through hole (i.e. without regard for the particular direction from which the signal trace intersects the via..

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Referring now to FIG. 11, a portion of a multi-connection via 124 embedded between layers of a multi-layer printed circuit board is shown. Such an embodiment is sometimes referred to as a "buried via." Although the buried via 124 is here shown providing connections between layer 125a, 125b, it should be appreciated that the via 124 could span more than two layers. The multi-connection via 124 includes a plurality of separate electrically isolated segments 126, each of which are connected to either a ground plane (not shown) or a signal trace (not shown) as required by the requisite circuitry of the printed circuit board to connect circuitry (not shown) on one layer to another layer.

With the use of the embedded multi-connection via 124, fewer vias are needed within the structure of the multi-layer printed circuit board to provide the same number of connections as can be made with conventional plated through holes. Thus the buried multi-connection via approach increases the connection density of the multi-layer printed circuit board. Furthermore, the buried multi-connection via approach eliminates electrical stubs from unused portions of vias thereby reducing or in some cases eliminating EMI above and below the board, and resin or some other appropriate sealant can be disposed in the via (by natural flow or by injection techniques) to seal exposed fiber edges in the split. Although not explicitly shown in FIG. 11, it should be appreciated that each of the segments 126 may have pads (such as pad 28a, 28b in FIG. 1A) coupled thereto to provide a means for contacting portions of ground or signal layers in the PCB.

Referring now to FIGS. 12 – 12E, signal routing techniques taking advantage of the inventive MCV are described. FIG. 12 shows known routing techniques with conventional PTHs or vias 130 to pass a signal from one layer of a printed circuit board (also referred to as a printed wiring it board) to another layer. Using conventional PTHs 130, first signal paths 132a enter the PTH 130 from a first

direction and second signal paths 132b enter the PTH 130 from a second direction which is orthogonal to the first direction. It should be noted that in each of FIGs. 12-12E, the traces enter the via on one layer and exit on another. It should also be noted that not all signal traces such as traces 132a are on the same layer nor are all signal
5 traces such as signal traces 132b on the same layer.

FIG. 12A shows a routing technique using four MCVs 134 to route signal paths 132a from one layer of the printed circuit board to another layer. In this embodiment, each of the MCVs 134 include a ground segment 136 which can be
10 connected to a ground plane layer on the printed circuit board and a signal segment 138 appropriately connected to signal paths 132a and 132b to route signals from the signal paths 132a and 132b. The signal paths 132a, 132b may each be on different layers of a multi-layer printed circuit board.

15 As shown in FIG 12B, the signal paths 132a, 132b can be routed using two MCVs 142a, 142b. Each of the MCVs includes a first and second signal segments 144, 148 and first and second ground segment 146, 150. Each of the ground segments 146, 150 is connected to the ground plane layer to provide a ground. The first signal segment 144 of MCV 142a is coupled to a pair of signal traces 132a, 132b to provide
20 a first signal path through the first MCV 142a and the second signal segment 148 is connected to a pair of signal traces 132a, 132b to provide a second signal path through the MCV 142a.

Similarly, the first signal segment 144 of MCV 142b is coupled to a pair of
25 signal traces 132a, 132b to provide a first signal path through the first MCV 142b and the second signal segment 148 is connected to a pair of signal traces 132a, 132b to provide a second signal path through the MCV 142b. It should be appreciated with such an arrangement, less vias need to be fabricated in the printed circuit board to provide a similar amount of signal paths, thus simplifying certain aspects of the

manufacturing requirements and processes, and increasing the space for routing the layers.

Referring to FIG. 12C, a prior art PTH 130' is used to route a pair of signal path 152a entering the PTH 130' from a first direction and a second pair of signal paths 152b entering the PTH 130 from a second direction which is aligned with the first direction.

FIG. 12D shows a routing technique using two MCVs 134' to route signal paths 152a from one layer of the printed circuit board to another layer. In this embodiment, each of the MCVs 134' include a ground segment 136' which can be connected to a ground plane layer on the printed circuit board and a signal segment 138' appropriately connected to signal paths 152a and 152b to route signals from the signal paths 152a and 152b. The signal paths 152a, 152b may each be on different layers of a multi-layer printed circuit board.

As shown in FIG 12E, the signal paths 152a, 152b can be routed using a single MCVs 142'. The MCV 142' includes first and second signal segments 144', 148' and first and second ground segment 146', 150'. Each of the ground segments 146', 150' are connected to a ground plane layer to provide a ground. The first signal segment 144' of MCV 142' is coupled to a pair of signal traces 152a, 152b to provide a first signal path through the MCV 142' and the second signal segment 148' is connected to a pair of signal traces 152a, 152b to provide a second signal path through the MCV 142'.

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It should be appreciated with such an arrangement, fewer vias are required in the multilayer printed circuit board. Thus, the MCV reduces the number of vias required in a printed circuit board providing the same functionality of multiple PTHs and also while conserving valuable area on the printed circuit board, simplifying

certain aspects of the manufacturing requirements (e.g. since fewer plated through holes are required) and processes and allowing increases in connection density of the printed circuit board. It should, however, be noted that splitting the via is an added step which may result in somewhat increased complexity in the manufacture of the PCB. In addition high speed performance characteristics are not attainable with conventional vias.

Referring now to FIGs. 13, 13A and 13B, having described various embodiments of a via with multiple conductors, it should now be appreciated, an improved multi-connection connector 160 including a first contact 162 and a second contact 164 can be provided to mate with a plated through hole or via 168 disposed within a printed circuit board 166. the via 168 having a first separate electrically segment 172 which mates with contact 162 and a second separate electrically isolated segment 174 which mates with contact 164. As shown in FIG. 13A, the via 168 can be arranged in a differential pair to provide two signal paths with segment 172 providing the first signal path and segment 174 providing the second signal path. Alternatively, as shown in FIG. 13B, the via 168 can be arranged with a signal segment 172' and a ground segment 174' to provide a single signal path. In this embodiment, contacts 162 and 164 press fit into the via 168 to provide connectivity between the connector 160 and the printed circuit board 166 as shown.

For differential connections, it is desirable to have a ground structure close to the differential pair. Usually referred to as a drain, this ground structure provides return to stray signals due to imperfections in the differential pair. FIGs. 13C and 13D shows an embodiment with connector elements that provide three connections required for a good differential pair. A pressfit connector 176 includes a first signal contact 178, a second signal contact 182 and a ground contact 180 that will mate with a plated through hole or via 186 disposed within a printed circuit board 184. The via 186 includes a first signal segment 188 which mates with contact 178, a second signal

segment 200 which mates with contact 182 and a ground segment 190 which mates with ground contact 180. The latter arrangement provides a ground path is close proximity to the signal path. A pressfit connection is shown but a soldered-in connector could also be used.

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Referring now to FIGs. 14 and 14A, scaling the number of connections to four per via provides for two single-ended signals and two ground segments separating them. In this embodiment, a connector 202 includes a first signal contact 204 and a second signal contact 208 and a pair of ground contacts 204. A via 212 disposed in the printed circuit board 210 includes a first signal segment 214 which mates with contact 204, a second signal segment 218 which mates with contact 208 and a first and second ground segment 216, 220. The pair of ground contacts 204 makes connections to the two opposite segments 216, 220 of the via 212 separating the two signal paths.

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FIGs. 15 and 15A show a variation of this configuration using known connector types, namely eye-of-the-needle pressfit contact 222 and pressure-mount pads 224, with a multi-connection via 212'. The pressfit contact 222 is press fit against segment 223 which provides the required retention force. It should be noted that the architecture shown in FIGs. 15, 15A illustrate a so-called "shielded via" concept which can be applied to existing products, with minor PCB routing redesign.

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Referring now to FIG. 16, a co-cylindrical waveguide 230 is shown having a similar structure as a co-planer waveguide 250. In the co-cylindrical waveguide 230, an interior wall 234 of a plated hole 232 which is a cylinder includes both a ground conductor 238 and a signal conductor 236. As in a co-planer waveguide 250 having a signal conductor 236' and a ground conductor 238', a signal propagates along the co-cylindrical waveguide 1681 between the signal conductor 236 and the adjacent ground conductor 238.

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A co-cylindrical waveguide provides a similar structure and maintains impedance control between signal and ground segments in a way analogous to a co-planar waveguide. Impedance matching is controlled by controlling diameter of the signal segment and signal arch length and gap relative to the ground segment and ground plane clearances. A typical embodiment often results in a small signal segment relative to the ground segment. When appropriate, the ground segment can be divided into more than one segment without performance degradation. In the case of one signal segment and one ground segment, the ground segment is typically, but not always, greater than 180 degrees.

Referring to FIG. 17, a differential via structure, here a co-cylindrical waveguide 240 having two signal segments 242, 244 among the ground segment 246 and typically the signal segments 242, 244 are much narrower than the ground segment 246. The impedance is matched by controlling diameter, signal segment arch lengths, gap spacing between signal segments, signal segment gap spacing relative to a ground segment and ground plane clearances. By providing separate signal segments 242, 244 and ground segment 246, a differential signal can be transmitted in a single via. Again, the differential co-cylindrical waveguide 240 has similar characteristics to a differential co-planar waveguide 240'. It should be noted that during the manufacturing process the ends of the glass fibers of the printed circuit board 239 may be exposed during the process to split the via into multiple segments. The via can be filled with a dielectric material (such as epoxy) to seal the ends of the glass fibers thereby preventing the fibers from absorbing moisture which could affect the performance of circuits disposed on the PCB and also reduce the structural integrity of the PCB..

Referring again to FIG. 16, it should be appreciated, the impedance, Z , of the co-cylindrical waveguide is a function of $Z = f(d_f, T_p, T_w, X_g, X_p, \epsilon_{r,board}, \epsilon_{r,via})$,

where: d_f = finished diameter, T_p = plating thickness, T_w = the gap, X_g = clearance in the ground plane, X_p = ground plane spacing, $\epsilon_{r,board}$ = dielectric constant of the PCB, and $\epsilon_{r,bourd}$ = dielectric constant inside the via. When the via diameter is very large, co-planer waveguide modeling provides a good approximation of the characteristics of a co-cylindrical waveguide until further models are developed exclusively for co-cylindrical waveguides. It should be noted that impedance values can be found using a variety of numerical techniques including but not limited to finite element techniques. The simplest co-planer waveguide case is the single-ended, infinite wide ground-conductor, and infinite thick substrate case, as depicted in FIG. 16, which also approximates the large diameter co-cylindrical waveguide, because the grounds connect together and the substrate is in the plane of the board making it very thick. The general approach to this analysis is to use a conformal imaging method as described below. The complete first order elliptical integral ($K(k)$) of the modulus w/d (equals k) as:

$$Z_{l,0} = \frac{Z_{l,0}}{\sqrt{\epsilon_{r,eff}}} = \frac{\eta_0 K(\sqrt{1-k^2})}{4\sqrt{\epsilon_{r,eff}} \cdot K(k)} \quad \text{Eq. D1}$$

In this case the thickness, t , is considered to be infinitely thin. η_0 is the permeability of free space (120π). The dielectric constant is averaged between the substrate and the air, yielding an effective dielectric constant:

$$\epsilon_{r,eff} = \frac{(\epsilon_r + 1)}{2} \quad \text{Eq. D2}$$

By dividing the bounds, the formulation can be fit into two, more useful cases. The first case is when $0 < w/d \leq 0.173$ or $\eta_0 \leq Z_{l,0} < \infty$:

$$Z_{l,0} = \frac{\eta_0}{2} \ln \left(2\sqrt{\frac{d}{w}} \right) \quad \text{Eq. D3}$$

Solving for modulus gives:

$$\frac{w}{d} = 4e^{-2Z_{l,0} \frac{\eta_0}{\pi}} \quad \text{Eq. D4}$$

be divided into more than one segment without performance degradation. In the case of one signal segment and one ground segment, the ground segment is typically, but not always, greater than 180 degrees. A differential via structure incorporates two signal segments among the ground segment and typically the signal segment is much narrower than the ground segment. The impedance is matched by controlling diameter, signal segment arc lengths, gap spacing between signal segments, signal segment gap spacing relative to a ground segment and ground plane clearances. By separating signal segments 266 with ground segments 264, multiple signals can be transmitted in a single via. It should be noted that during the manufacturing process the ends of the glass fibers of the printed circuit board 254 may be exposed. The via can be filled with a dielectric material (such as epoxy) to seal the ends of the glass fibers.

It should now be appreciated a different signal can be transmitted on each one of the signal segments 266 and that the surface mount device 250 can be disposed on the printed circuit board 254 with connector 280 utilizing much less surface of the printed circuit board 254 as needed when using known vias.

Referring now to FIGs. 19 and 19A, a pressfit and SMT hybrid connector 300 is shown. A surface mount device 310 is shown with a plurality, here two, of surface mount technology (SMT) contacts 302. A printed circuit board 304 includes a multi-connection via 320, here including four separate segments 322, where the surface mount device 310 is mounted. A plurality, here two, of SMT pads 314 are disposed on the printed circuit board 304 as shown to receive corresponding ones of the SMT contacts 302. A pressfit contact 316 is disposed between the SMT contacts 302 as shown. Here, the pressfit contact 316 provides a ground conductor as well as the required retention force and the SMT contacts 302 provide signal conductors. With such an arrangement, the connector 300 provides a signal path for two signals.

Referring now to FIG. 20, a SMT connector 400 is shown. An SMT by-pass capacitor 410 is shown with two SMT contacts 402. A printed circuit board 404 includes a multi-connection via 420, here including two separate segments 422. Two SMT pads 414 are disposed on the printed circuit board 404 as shown to receive

5 corresponding ones of the SMT contacts 402. Here, one of the separate segments 422 provides a ground conductor and the other one of the separate segments 422 provides a signal conductor or here a power conductor. With such an arrangement, the connector 400 provides a signal path to connect the SMT by-pass capacitor 410 to the printed circuit board 404. In a typical SMT by-pass capacitor, the lead length from the

10 power and ground planes determines the lead inductance. The shorter the lead, the lower the inductance will be, and consequently, the higher the frequency of operation. Utilizing a multi-connection via connector does not change the design of the SMT package of the by-pass capacitor, but takes advantage of the new via geometry for routing only. Placing the via directly below the SMT by-pass capacitor 402, as shown

15 in FIG. 20, reduces the inductance loop to only the surface trace. Because the via itself offers an impedance-controlled structure, the inductance caused by a conventional via configuration does not apply. The offers a superior solution than using micro-vias because power planes most often are located in the middle of the printed wiring board, where micro vias cannot easily reach.

20 Referring now to FIGs. 21 and 21A, a printed circuit board 510 is shown to include a plurality of SMT connectors 500 each having a multi-connection via 520 adapted to connect to a daughter board connector, represented here as a collection of SMT wafers 505. It should be appreciated that although MCV 520 is here shown

25 providing connections to a plurality of SMT daughter board wafers, those of ordinary skill in the art will recognize that MCVs 520 may be used to couple any type of PCBs.

Each one of the SMT connectors 500 include an SMT pad 502 to provide a ground connection and an SMT pad 504 to provide a signal connection. In a similar

manner as described earlier, the multi-connection via 520 includes a ground segment 506 to provide a ground conductor connected to a corresponding SMT pad 502 and a signal segment 508 to provide a signal conductor connected to a corresponding SMT pad 504. Each of the SMT pads 502 are connected together with the ground segments 506 as shown.

For each one of the SMT pads 502, an SMT contact 552 is located on the daughter board connector wafer 505 to mate with a corresponding SMT pad 502 as shown to provide a ground connection between the daughter board 505 and the printed circuit board 510. For each one of the SMT pads 504, an SMT contact 554 is located on the daughter board connector wafer 505 to mate with a corresponding SMT pad 504 as shown to provide a signal connection between the daughter board connector wafer 505 and the printed circuit board 510. It should now be appreciated with such an arrangement, when using the SMT connectors 500, fewer vias are required on the printed circuit board 510 to provide a similar number of connections between the daughter board 505 and the printed circuit board 510. The latter provides better routability of signal paths between the daughter boards 505 and the printed circuit board 510. Such an arrangement also provides better signal integrity for high speed circuits i.e. less cross talk, eliminates reflections, reduced attenuation and in general provides better impedance control of the signal path between the daughter board connector wafer 505 and the printed circuit board 510. It should also be appreciated that more connections between the daughter board connectors 505 and the printed circuit board 510 can be made with the SMT connectors 500 within the same amount of space than when using known via structures (assuming that microvias are not being considered).

Referring now to FIGs. 22 and 22A, a printed circuit board 610 is shown to include a plurality of SMT connectors 600 each having a differential multi-connection via 620 for connecting a daughter board connector, represented here as a collection of

SMT wafers 605. It should be noted that connectors shown in FIG. 22 are also described in co-pending application no. 09/198,442 assigned to the assignee of the present invention and incorporated herein by reference.

5 It should be noted that although daughter board connectors are here shown, any type of connector a could also be used. Each one of the SMT connectors 600 include an SMT pad 602 to provide a ground connection and SMT pads 604a and 604b to provide a differential signal connection.

10 The multi-connection via 620 includes a ground segment 606 to provide a ground conductor connected to a corresponding SMT pad 602, a signal segments 608 and 609 to provide a differential signal conductor connected to corresponding SMT pads 604a and 604b. Each of the SMT pads 602 are connected together with the ground segments 606 with other SMT pads 603 disposed between the SMT pads 602
15 as shown.

 The multi-connection via 620 includes two signal conductors providing differential signal path for corresponding signal. For each one of the SMT pads 602, an SMT contact 652 is located on the daughter board connector wafer 605 to mate
20 with a corresponding SMT pad 602 as shown to provide a ground connection between the daughter board connector wafer 605 and the printed circuit board 610. Additionally, an SMT contact 653 located on the daughter board connector wafer 605 provides a ground connection between the daughter board and the printed circuit board 610 mating with SMT pads 603. For each one of the SMT pads 604a, an SMT
25 contact 654 is located on the daughter board connector wafer 605 to mate with a corresponding SMT pad 604a as shown to provide a signal connection between the daughter board connector wafer 605 and the printed circuit board 610. For each one of the SMT pads 604b, an SMT contact 655 is located on the daughter board connector wafer 605 to mate with a corresponding SMT pad 604b as shown to provide

a signal connection between the daughter board 605 and the printed circuit board 610.

5 It should now be appreciated with such an arrangement, when using the SMT connectors 600, fewer vias are required on the printed circuit board 610 to provide a similar number of connections between the daughter board 605 and the printed circuit board 610. The latter provides better routability of signal paths between the daughter boards connector wafer 605 and the printed circuit board 510 as well as routability between rows, which is not possible with conventional vias. It should also be
10 appreciated that conventional via structures do not provide a true differential connection between layers in the PCB, thus this arrangement provides a superior performing connection from the daughter card connector to the layer trace.

Referring now to FIG. 23, an alternative embodiment of printed circuit board
15 610 is shown to include a plurality of SMT connectors 600' each having a multi-connection via 620 provided in the printed circuit board 610. In the alternative embodiment, an additional via 670 connected to a pad 671 is included to provide a ground connection and replacing the surface traces of the previous embodiment. It should be noted that the embodiment of FIG. 23 is similar to the same differential
20 configuration as the embodiments of FIGs. 21-22 but instead of a surface trace connecting the additional ground pin (specific to the connector illustrated) a separate conventional ground via is used.

In present vias, the metal plating of the via acts to seal the cut drilled surface
25 of the via. In fabricating multi-connection vias, drilling exposes cut ends of the glass fiber of the printed wiring board, allowing the printed circuit board to absorb moisture and other chemicals. Cutting the plating to form a split via exposes the fibers again. In all of the embodiments showing a multi-connection via, the via can be filled with a dielectric material (such as epoxy) to seal the ends of the glass fibers exposed between

the conducting material. For pressfit contacts a soft gel seal can be used which will push out of the way of the connector as it is pressed into the hole to seal the ends of the glass fibers exposed between the conducting material.

5 It should now be appreciated that various connectors can be contemplated, for example, referring now to FIGs. 2 - 3E any one of the multi-connection vias shown could be adapted to provide an appropriate multi-connection connector.

10 It should be appreciated that multi-connection vias, described herein, provide a structure and method for matching the impedance of vertical and in-plane features by forming co-cylindrical waveguides. Solutions from a high-frequency full-wave solver provide insight into field interactions within multi-connection vias; and results from these simulations and signal integrity experiments indicate impedance "tuneability" by adjusting the multi-connection via dimensions. The results also suggest that features
15 can be impedance-matched independent of via diameter.

 All references cited herein are hereby incorporated herein by reference in their entirety.

20 Having described preferred embodiments of the invention, it will now become apparent to one of ordinary skill in the art that other embodiments incorporating their concepts may be used. It is felt therefore that these embodiments should not be limited to disclosed embodiments, but rather should be limited only by the spirit and scope of the appended claims.

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What is claimed is:

Claims

- 1 1. An interconnection structure for providing a signal path between a first layer
2 and a second different layer of a multi-layer structure, the interconnection structure
3 comprising a plated through hole having a plurality of electrically isolated segments
4 with at least one of the plurality of electrically isolated segments coupled to one of a
5 signal path and a circuit component and at least one of the electrically isolated
6 segments coupled to a ground plane layer of the multi-layer structure.
- 1 2. The interconnection structure of Claim 1 wherein each of the plurality of
2 electrically isolated segments coupled to signal paths are provided having equal
3 widths and each of the at least one of the electrically isolated segments coupled to
4 ground are provided having equal widths.
- 1 3. The interconnection structure of Claim 1 wherein at least two of the plurality
2 of electrically isolated segments are coupled to signal paths and are provided having
3 different widths.
- 1 4. The interconnection structure of Claim 1 wherein at least two of the plurality
2 of electrically isolated segments are coupled to the ground plane layer of said multi-
3 layer structure and are provided having different widths.
- 1 5. The interconnection structure of Claim 1 wherein the at least one of the
2 plurality of electrically isolated segments which is coupled to a signal path has a width
3 which is less than the width of the at least one of the electrically isolated segments
4 coupled to the ground plane layer of said multi-layer structure.

1 6. The interconnection structure of Claim 1 wherein said plurality of electrically
2 isolated segments of said plated through hole are disposed in a symmetric pattern
3 about a central longitudinal axis of said plated through hole.

1 7. The interconnection structure of Claim 1 wherein said plurality of electrically
2 isolated segments of said plated through hole are disposed in an asymmetric pattern
3 about a central longitudinal axis of said plated through hole.

1 8. The interconnection structure of Claim 1 wherein said plated through hole is
2 provided having a cross-sectional shape which is substantially round.

1 9. The interconnection structure of Claim 1 wherein said plated through hole is
2 provided having a cross-sectional shape which is substantially rectangular.

1 10. The interconnection structure of Claim 3 wherein said plated through hole is
2 provided having a cross-sectional shape which is substantially square.

1 11. The interconnection structure of Claim 1 wherein said plated through hole is
2 provided having an irregular cross-sectional shape.

1 12. The interconnection structure of Claim 1 wherein each of the plurality of
2 electrically isolated segments are provided having substantially equal widths.

1 13. A interconnection structure for providing a signal path between a first signal
2 trace on a first layer of a multi-layer structure and a second signal trace on a second
3 different layer of the multilayer structure, the interconnection structure comprising:
4 (a) a first electrically conductive path extending in a substantially vertical
5 direction along a surface of an opening in the multi-layer structure between the first
6 layer and the second layer of the multi-layer structure; and

7 (b) a second electrically conductive path extending in a substantially vertical
8 direction along the surface of the opening in the multi-layer structure between the first
9 layer and the second layer of the multi-layer structure and electrically isolated from
10 the first electrically conductive path, wherein a first one of the first and second
11 electrically conductive paths is coupled to the first and second signal traces and a
12 second one of the first and second electrically conductive paths is coupled to a
13 reference potential.

1 14. The interconnection structure of Claim 13 wherein the arc lengths of the first
2 and second electrically conductive paths are selected such that the interconnection
3 structure is provided having a predetermined electrical impedance characteristic.

1 15. The interconnection structure of Claim 14 wherein the multi-layer structure
2 includes a plurality of ground plane layers each of the which is provided from a
3 conductive material a portion of which has been removed from the region of the
4 ground plane layer proximate the location of the one of the electrically conductive
5 paths coupled to the first and second signal traces.

1 16. The interconnection structure of Claim 15 wherein the ground plane layer is
2 provided having conductive material in an asymmetrical pattern around the one of the
3 electrically conductive paths coupled to the first and second signal traces.

1 17. The interconnection structure of Claim 13 further wherein the first electrically
2 conductive path is coupled to the first and second signal traces, the second electrically
3 conductive path is coupled to ground and the interconnection structure further
4 comprises a third electrically conductive path extending in a substantially vertical
5 direction between the first layer and the second layer of the multilayer structure and is
6 coupled to third and fourth signal traces of the multi-layer structure.

1 18. A circuit comprising:
2 a first plurality of multi-connection vias arranged to provide a first cluster of
3 signal connection regions, each of the first plurality of multi-connection vias having at
4 least one segment coupled to ground; and
5 a second plurality of multi-connection vias arranged to provide a second
6 cluster of signal connection regions, each of the second plurality of multi-connection
7 vias having at least one segment coupled to ground and wherein said second plurality
8 of multi-connection vias are disposed in relation to said first plurality of multi-
9 connection vias to define a plurality of distinct routing channels between the first and
10 second clusters of signal connection regions.

1 19. The circuit of Claim 18 wherein:
2 the first plurality of multi-connection vias are disposed such that the ground
3 segments are juxtaposed; and
4 the second plurality of multi-connection vias are disposed such that the ground
5 segments are juxtaposed.

1 20. The circuit of Claim 18 wherein at least some of said first and second plurality
2 of multi-connection vias are provided as differential multi-connection vias having a
3 first pair of signal segments adapted to coupled to a first differential pair of signal
4 paths and a second pair of signal segments adapted to couple to a second differential
5 pair of signal paths wherein said first pair of signal paths are on a first layer of a multi-
6 layer printed circuit board and the second pair of signal paths are on a second different
7 layer of the multi-layer printed circuit board.

1 21. The circuit of Claim 18 wherein at least some of said first plurality of multi-
2 connection vias have a plurality of signal segments.

1 22. The circuit of Claim 18 wherein at least some of said first plurality of
2 multi-connection vias have a plurality of signal segments and a plurality of ground
3 segments.

1 23. The interconnection structure of Claim 1 further comprising at least one pad
2 coupled to each of said plurality of electrically isolated segments wherein each of said
3 pads is provided having one of a radial shape or a parallel shape.

1 24. A multi-connection via provided in a printed circuit board having a plurality of
2 signal layers and a plurality of ground layers, the multi-connection via comprising a
3 plated through hole provided in the printed circuit board, said plated through hole
4 having a first plurality of separate electrically isolated segments, with at least one of
5 the first plurality of electrically isolated segments adapted to couple to one of a
6 signal path and a circuit component and at least one of the first plurality of electrically
7 isolated segments adapted to couple to at least one of the plurality of ground plane
8 layers of the printed circuit board, wherein the widths of each of the at least one of the
9 plurality of electrically isolated segments adapted to couple to one of a signal path
10 and a circuit component and the at least one of the electrically isolated segments
11 adapted to couple to at least one of the plurality of ground plane layers of the printed
12 circuit board are selected to provide the multi-connection via having a predetermined
13 impedance characteristic.

1 25. The multi-connection via of Claim 24 wherein said plated through hole has a
2 first segment corresponding to a first signal segment which is adapted to couple to a
3 first signal trace and a second segment corresponding to a first ground segment which
4 is adapted to couple to one of the plurality of ground plane layers of the printed circuit
5 board.

1 26. The multi-connection via of Claim 25 wherein the first signal segment is a first
2 one of a plurality of signal segments and the first ground segment is a first one of a
3 plurality of ground segments.

1 27. The multi-connection via of Claim 25 further comprising a second signal
2 segment wherein said first and second signal segments are adapted to receive a
3 differential signal pair.

1 28. The multi-connection via of Claim 27 wherein the first and second signal
2 segments correspond to first ones of a plurality of pairs of differential signal segments.

1 29. The multi-connection via of Claim 24 further comprising a second plurality of
2 separate electrically isolated segments provided in said plated through hole, with at
3 least one of the second plurality of electrically isolated segments adapted to coupled to
4 at least one the ground plane layers of the printed circuit board.

1 30. The multi-connection via of Claim 29 wherein the first plurality of separate
2 electrically isolated segments are disposed in said plated through hole above said
3 second plurality of separate electrically isolated segments such that first ends of the
4 first plurality of separate electrically isolated segments are spaced by a predetermined
5 distance from second ends of the second plurality of separate electrically isolated
6 segments.

1 31. The multi-connection via of Claim 24 wherein each of said first plurality of
2 segments are provided having a split around a circumferential axis of said plated
3 through hole to provide the multi-connection via having first and second multi-
4 connection via portions.

1 32. A interconnection device for providing a signal path between a first layer and a
2 second different layer of a multilayer structure, the interconnection device comprising
3 a plated through hole having a first continuous nonconductive region provided therein
4 to define a first region of the plated through hole corresponding to a via trace segment
5 and a second region of the plated through hole corresponding to a ground trace
6 segment wherein said via trace segment is electrically isolated from the ground trace
7 segment and is adapted to couple to a signal path.

1 33. The interconnection device of Claim 32 wherein said signal path traverses in a
2 direction which is not vertical with respect to a central longitudinal axis of the via.

1 34. The interconnection device of Claim 32 wherein the first continuous
2 nonconductive region is a first one of a plurality of continuous nonconductive regions,
3 each of said plurality of continuous nonconductive regions defining a like plurality of
4 regions in the plated through hole corresponding to via trace segments wherein each
5 of said plurality of via trace segments are electrically isolated from the ground trace
6 segment and each of said plurality of via trace segments are adapted to couple to a
7 signal path.

1 35. An interconnection structure for providing a signal path between a first layer
2 and a second different layer of a multi-layer structure which includes a plurality of
3 signal layers and a plurality of ground layers, the interconnection structure
4 comprising:

5 a plated through hole having a first end, a second end and a plurality of
6 electrically isolated segments extending from the first end of the plated through hole
7 to the second end of the plated through hole with at least one of the plurality of
8 electrically isolated segments coupled to at least one of the plurality of signal layers of
9 the multi-layer structure and at least one of the electrically isolated segments coupled
10 to at least one of the plurality of ground layers of the multi-layer structure;

11 a first layer disposed over the first end of the plated through hole such that the
12 first end of the plated through hole is not exposed through the first layer; and
13 a second layer disposed over the second end of the plated through hole such
14 that the second end of the plated through hole is not exposed through the second layer.

1 36. The multilayer structure of Claim 36 wherein the widths of each of the
2 plurality of electrically isolated segments is selected such that the segments coupled to
3 signal layers are provided having a predetermined impedance characteristic.

1 37. The multilayer structure of Claim 36 wherein at least some of the plurality of
2 electrically isolated segments are coupled to a pad on one of the signal or ground
3 layers of the multi-layer structure.

1 38. The multilayer structure of Claim 35 wherein said plated through hole includes
2 a surface corresponding to exposed portions of a dielectric and said plated through
3 hole is filled with a material which reduces the amount of moisture absorbed by the
4 exposed portions of the dielectric in said plated through hole.

1 39. A multilayer structure comprising:
2 a plurality of ground layers;
3 a plurality of signal layers;
4 a first signal trace disposed on a first layer of said plurality of signal layers;
5 a second signal trace disposed on a second different layer of said plurality of
6 signal layers;
7 a plurality of support layers for structurally supporting said plurality of signal
8 layers and ground layers;
9 a multi-connection via having a first ground segment coupled to one of said
10 plurality of ground plane layers, a first signal segment having first portion coupled to
11 said first signal trace and having a second portion coupled to said second signal trace.

1 40. The multi-layer structure of Claim 39 further comprising a third signal trace
2 disposed on a third layer of said plurality of signal layers and a fourth signal trace
3 disposed on a fourth layer of said plurality of signal layers and wherein said a multi-
4 connection via includes a second ground segment coupled to one of said plurality of
5 ground plane layers and a second signal segment having a first portion coupled to said
6 third signal trace and having a second portion coupled to said fourth signal trace.

1 41. The structure of Claim 40 wherein said first and second signal segments and
2 said first and second ground segments of said multi-connection via are
3 disposed in a symmetric pattern about a longitudinal central axis of said multi-
4 connection via.

1 42. The multi-layer structure of Claim 41 wherein said first and second signal
2 traces are orthogonally disposed with respect to said multi-connection via.

1 43. The multi-layer structure of Claim 41 wherein said first and second signal
2 traces are aligned along a horizontal axis through said multi-connection via.

1 44. A circuit comprising:
2 a multilayer structure having a multi-connection via, said multi-connection via
3 having first and second electrically isolated segments and a predetermined spacing
4 between the first and second segments; and
5 a connector having first and second contacts spaced by a predetermined
6 distance and adapted to be disposed in said multi-connection via, said first and second
7 contacts are disposed against the first and second segments of said multi-connection
8 via.

1 45. The circuit of Claim 44 wherein:

2 said connector is provided having at least one ground conductor and a plurality
3 of signal conductors; and

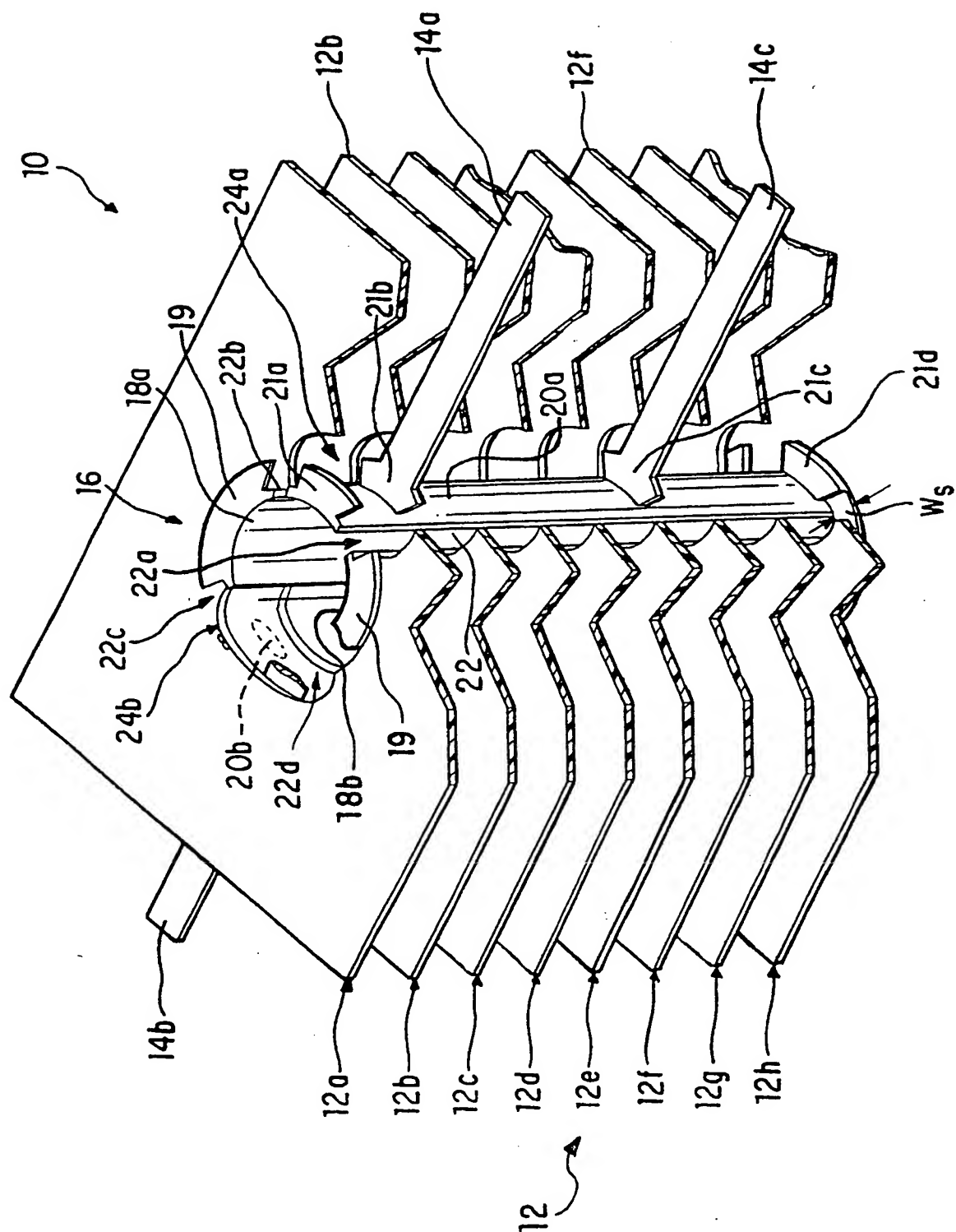
4 said multi-connection via includes at least one ground segment and a like
5 plurality of electrically isolated signal segments, wherein the signal segments are
6 provided having a size and spacing adapted to coupled to the plurality of signal
7 conductors of said connector.

1 46. The circuit of Claim 44 wherein

2 said connector is provided having an eye-of-the- needle connector disposed in
3 the multi-connection via such that a first portion of the eye of needle connector
4 contacts a first electrically isolated segment of the multi-connection via and a second
5 portion of the eye of needle connector contacts a second different electrically isolated
6 segment of the multi-connection via.

1 47. The circuit of Claim 46 wherein the first electrically isolated segment of the
2 multi-connection via is coupled to ground and the second different electrically isolated
3 segment of the multi-connection via is coupled to a signal line.

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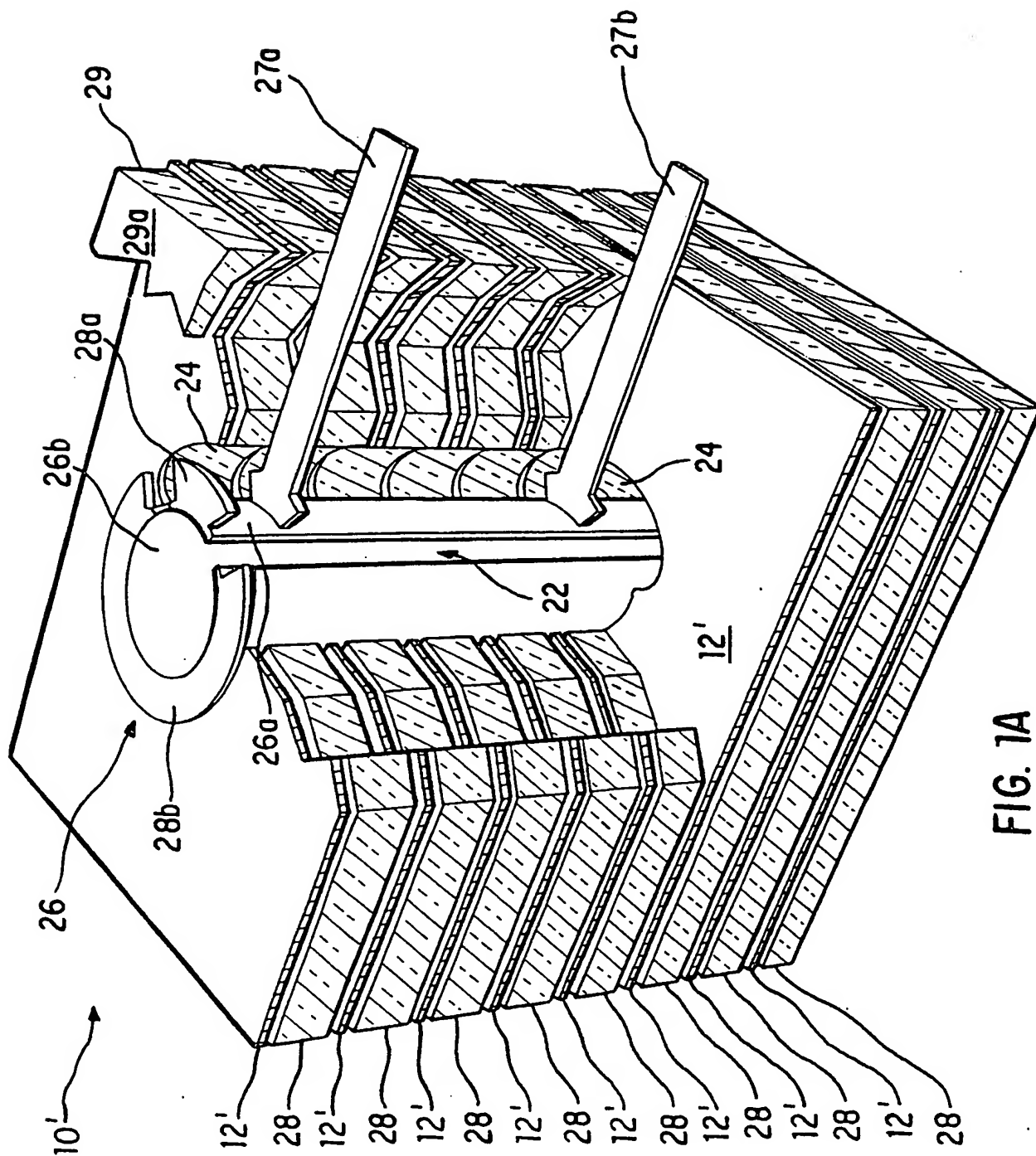


FIG. 1A

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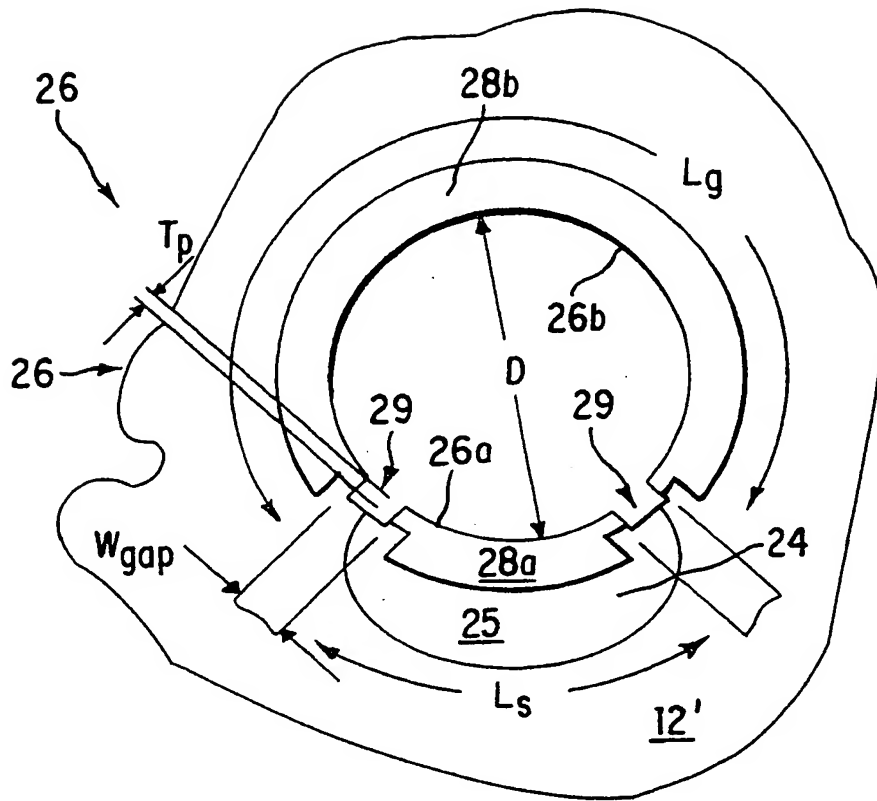


FIG. 1B

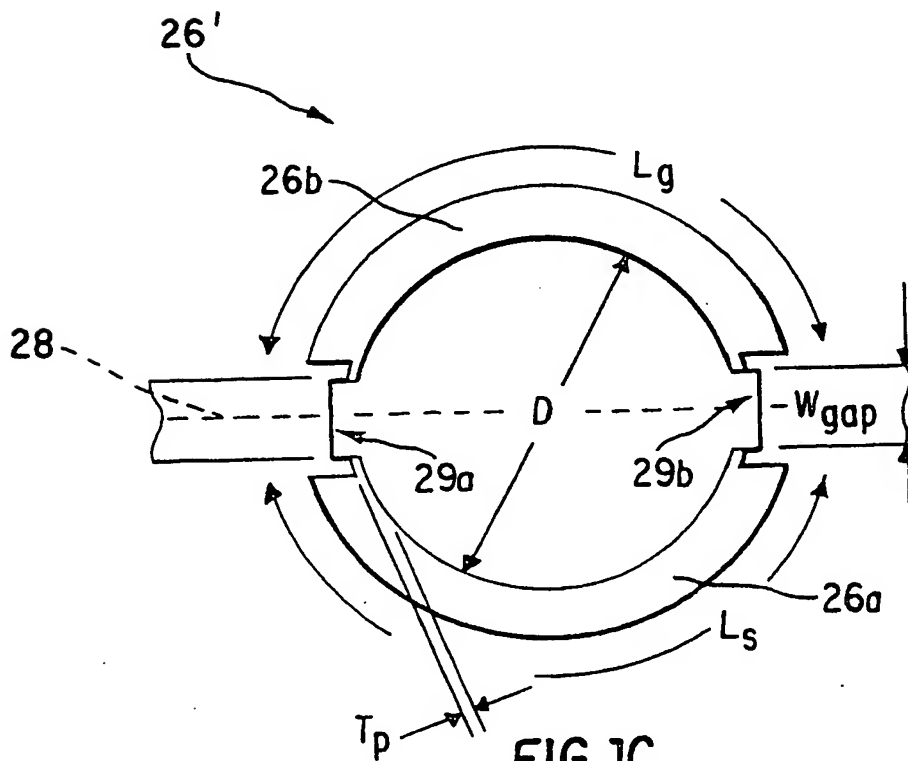


FIG. 1C

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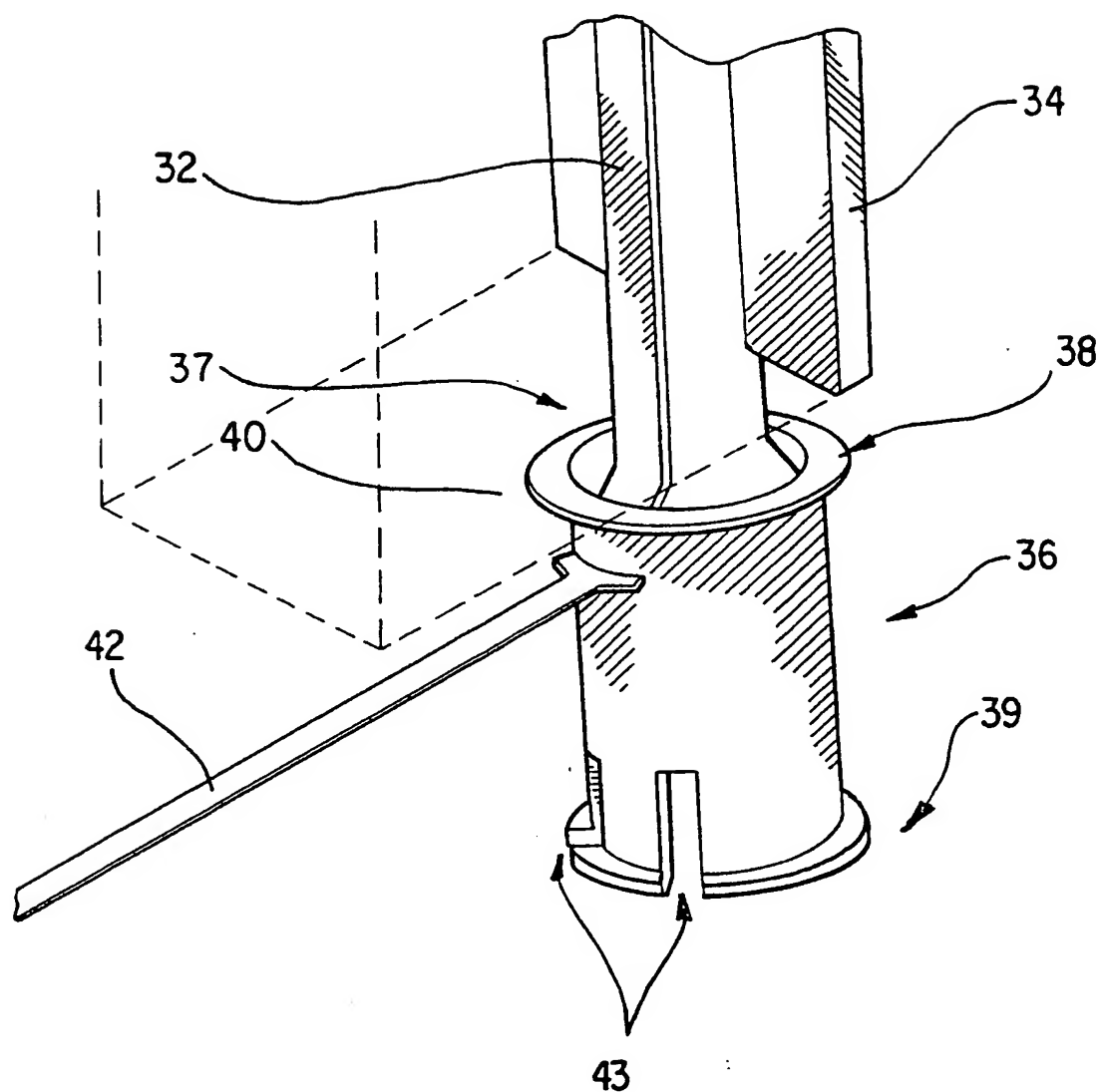


FIG. 1D

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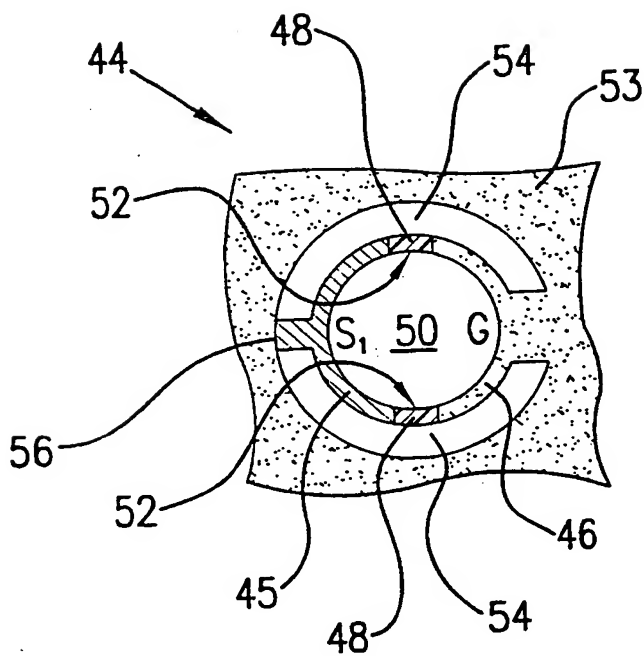


FIG. 2

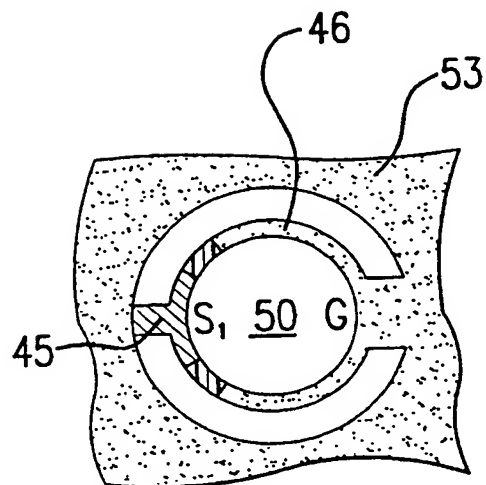


FIG. 2A

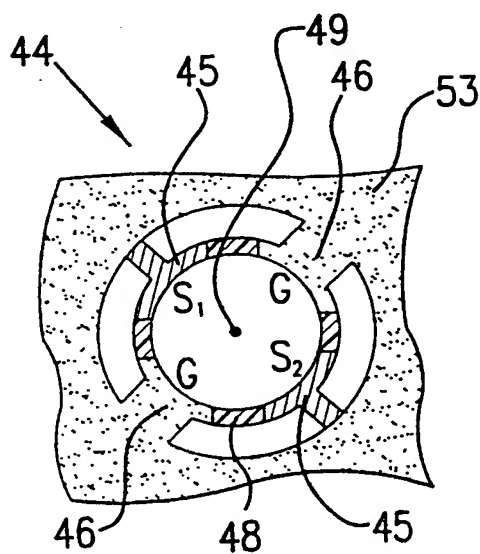


FIG. 2B

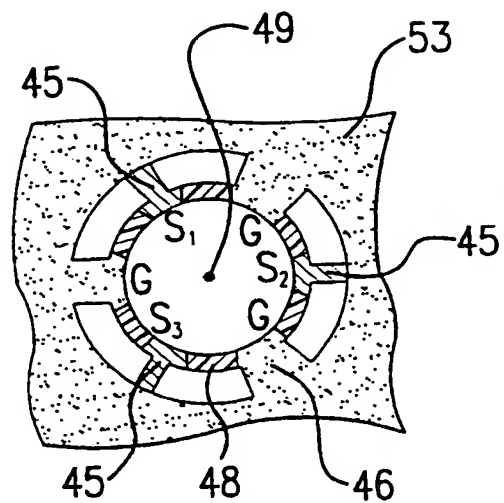


FIG. 2C

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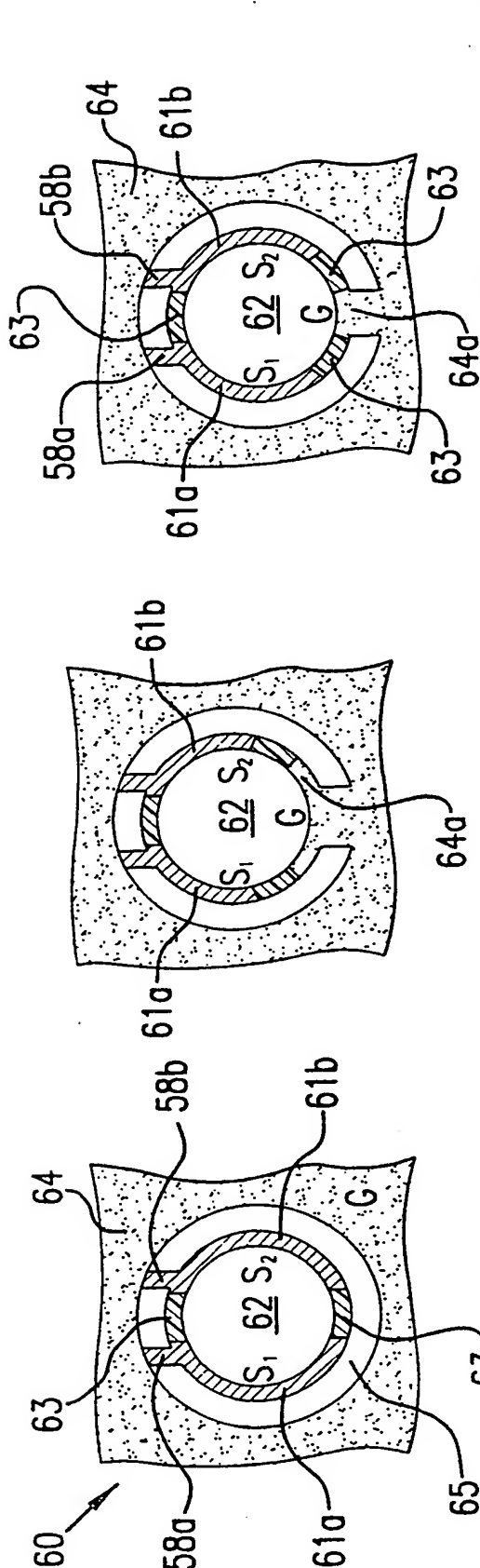


FIG. 3B

FIG. 3A

FIG. 3

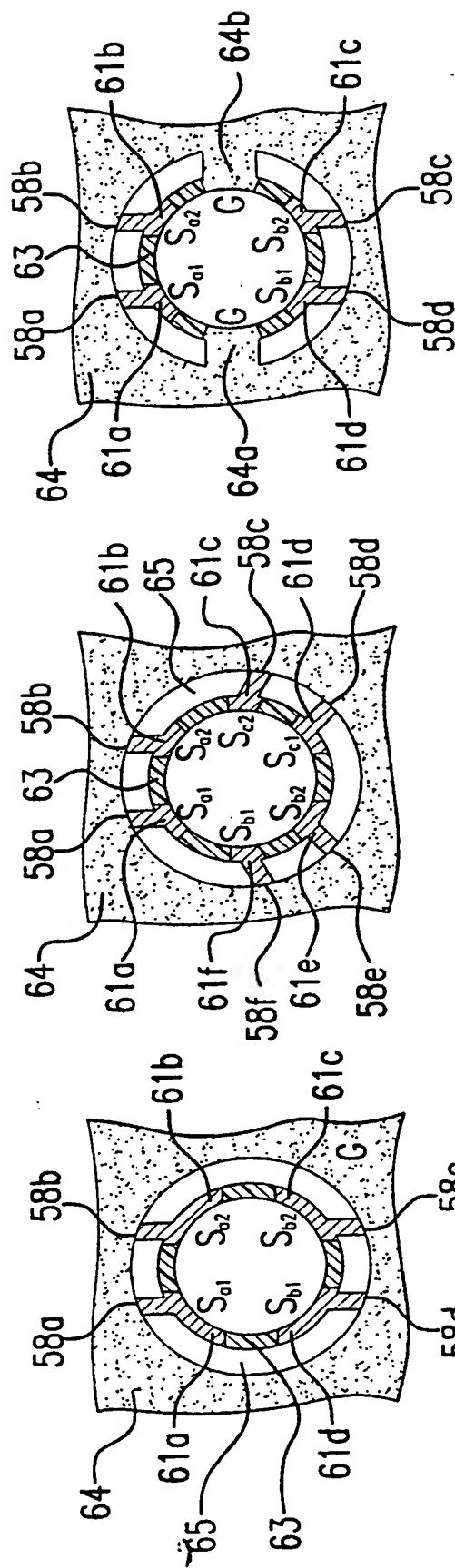


FIG. 3E

FIG. 3D

FIG. 3C

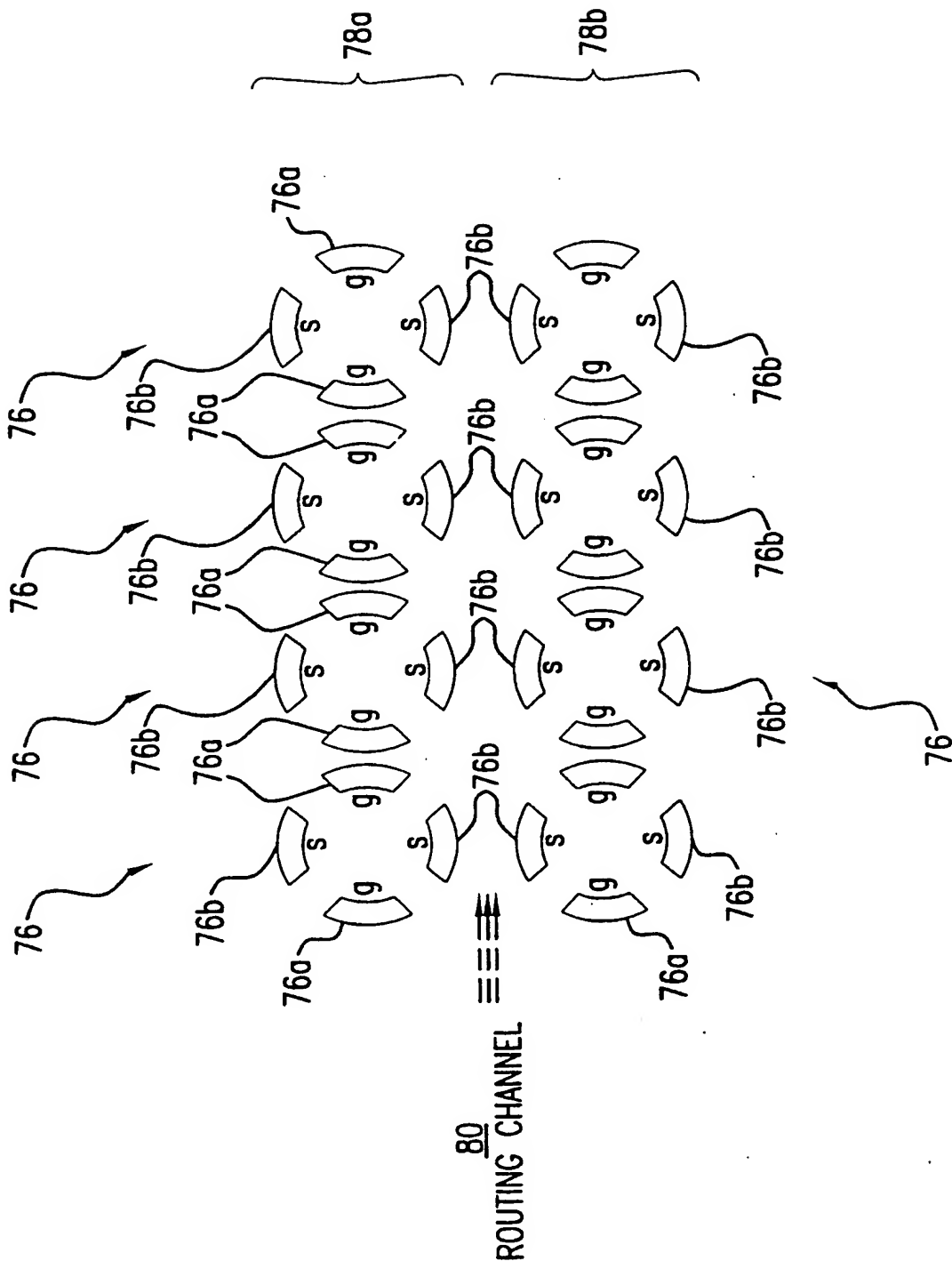


FIG. 4B

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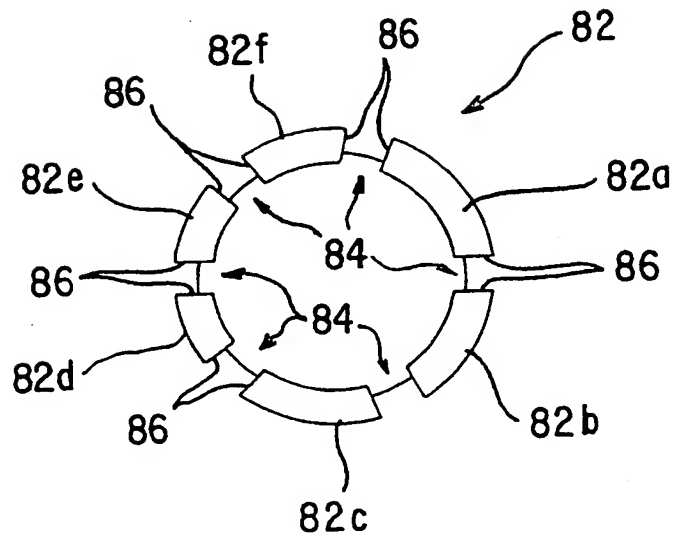


FIG. 5

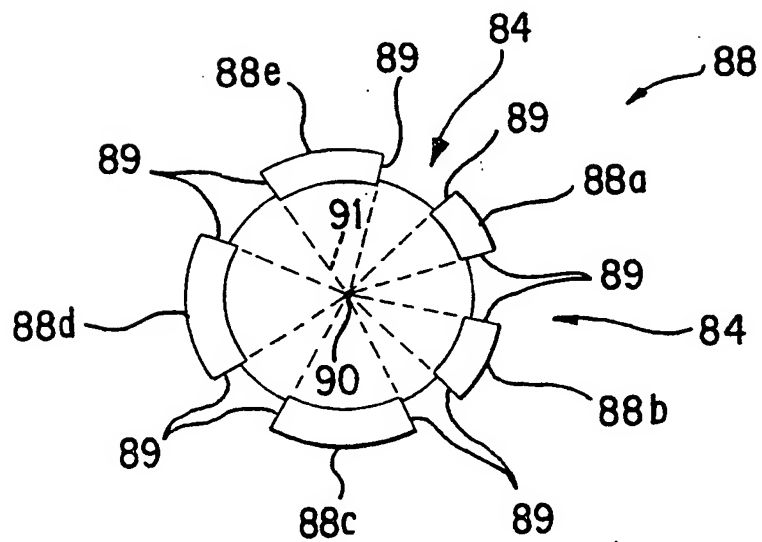
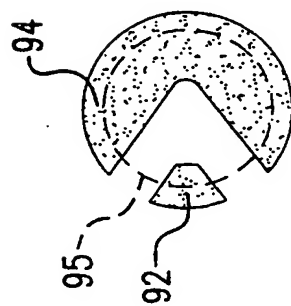
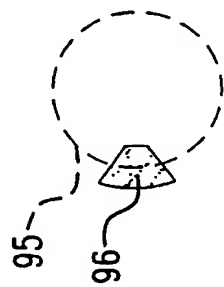


FIG. 6

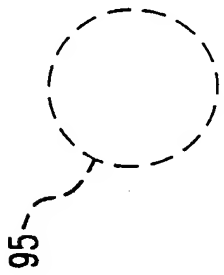
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TOP AND BOTTOM
PAD LAYERS



SIGNAL LAYERS WITH
TRACE TO VIA



SIGNAL LAYERS
WITHOUT TRACE TO VIA

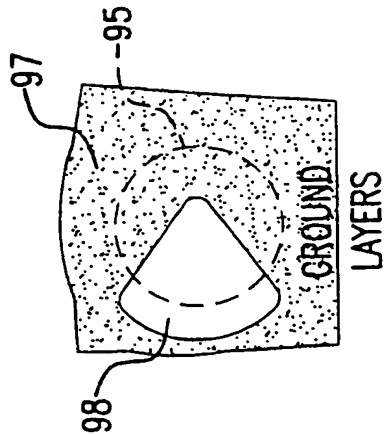
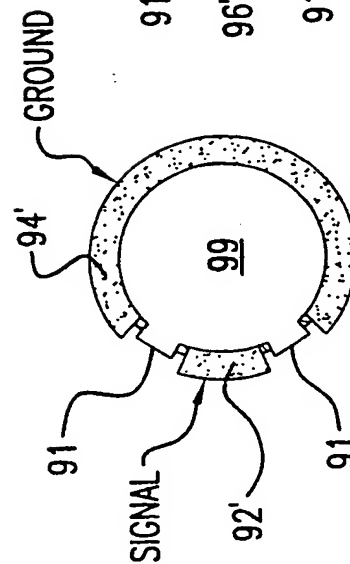


FIG. 7

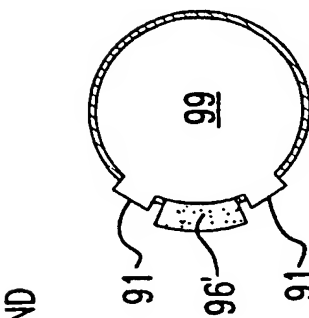
FIG. 7A

FIG. 7B

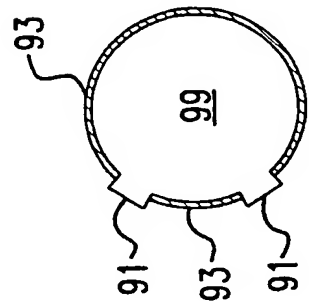
FIG. 7C



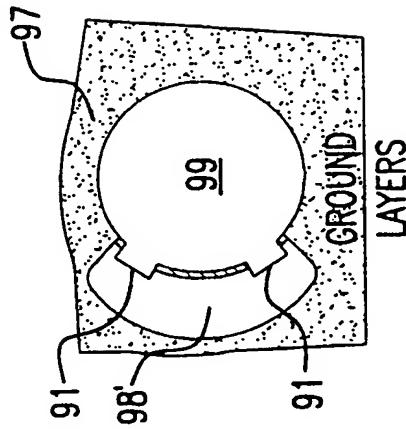
TOP AND BOTTOM
PAD LAYERS



SIGNAL LAYERS WITH
TRACE TO VIA



SIGNAL LAYERS
WITHOUT TRACE TO VIA



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FIG. 8

FIG. 8A

FIG. 8B

FIG. 8C

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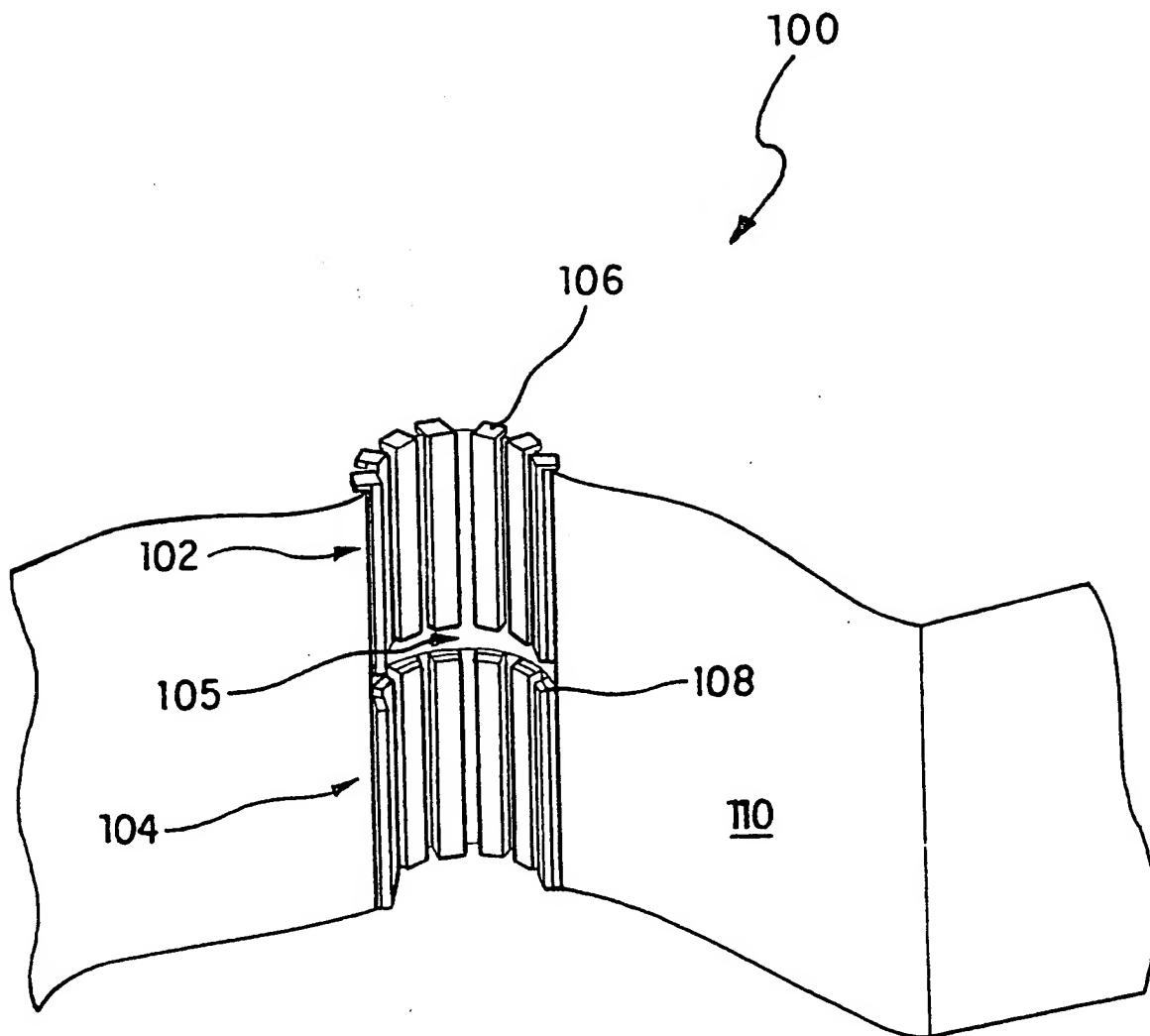


FIG. 9

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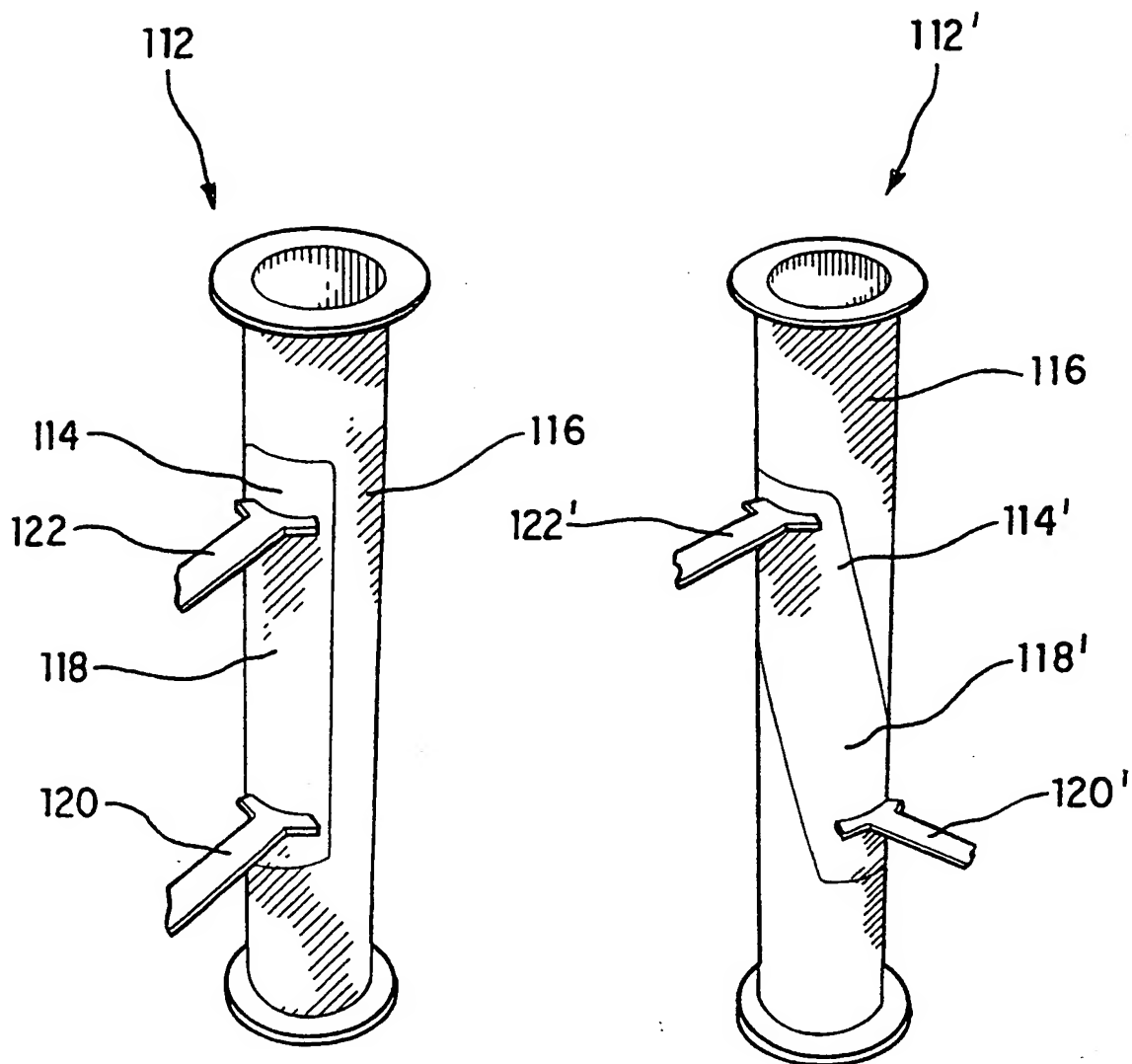


FIG. 10

FIG. 10A

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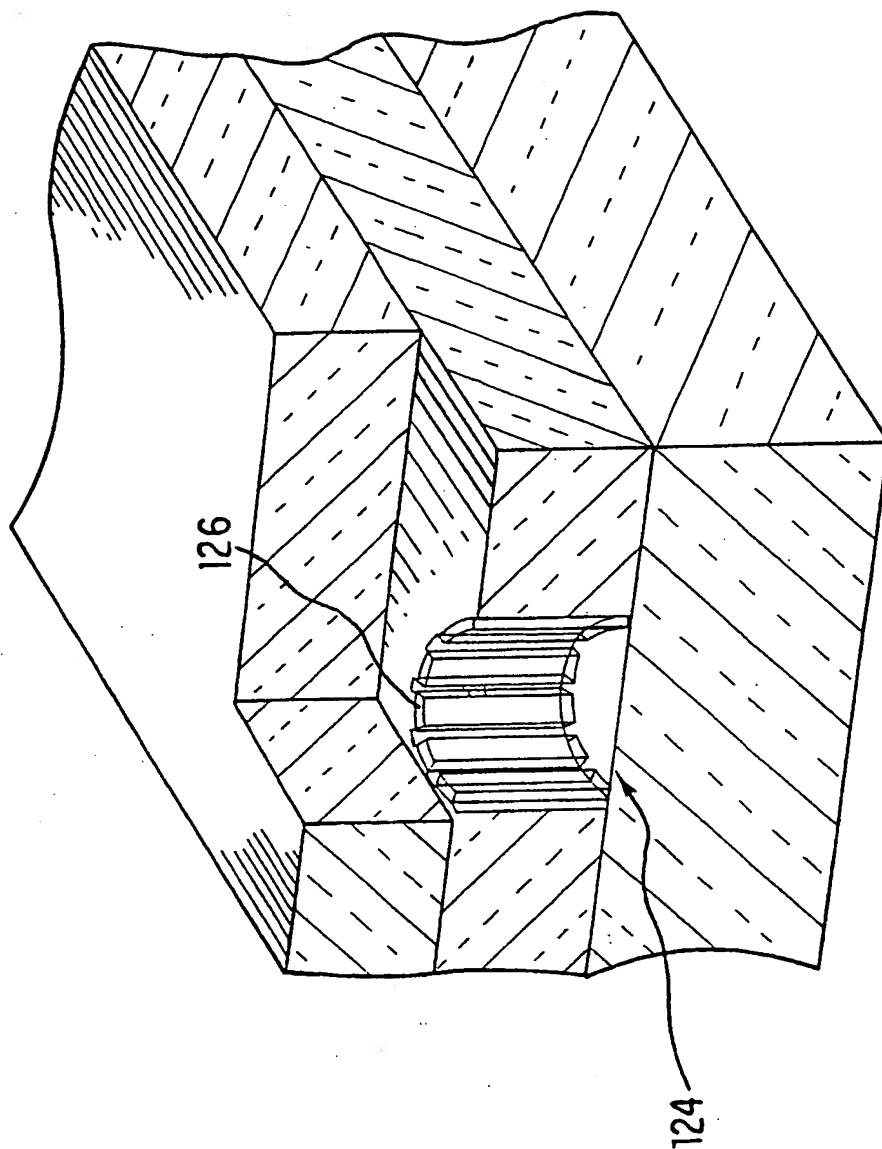


FIG. 11

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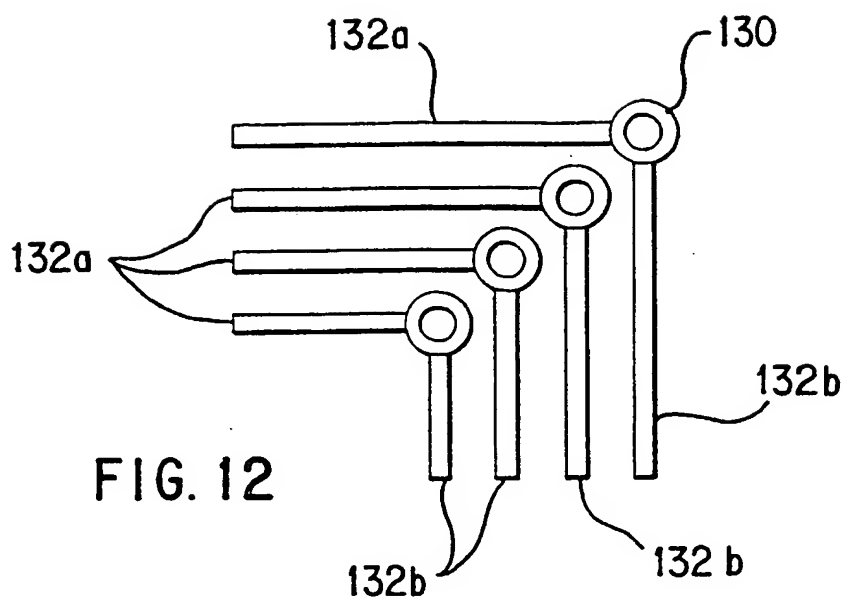


FIG. 12

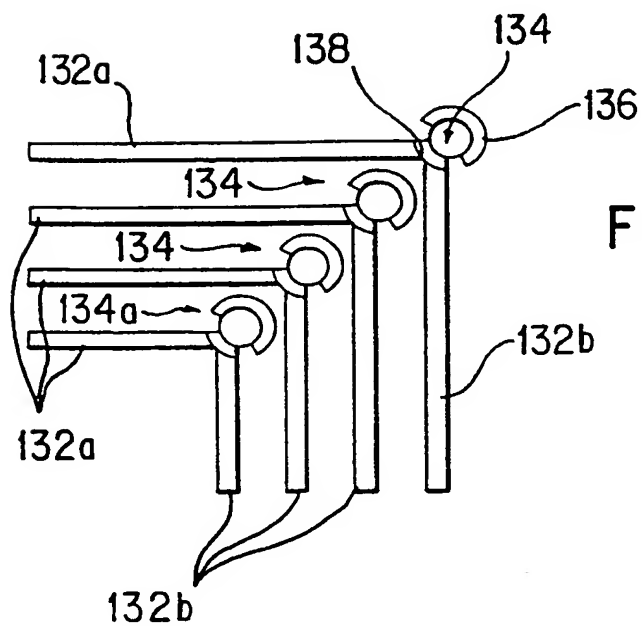


FIG. 12A

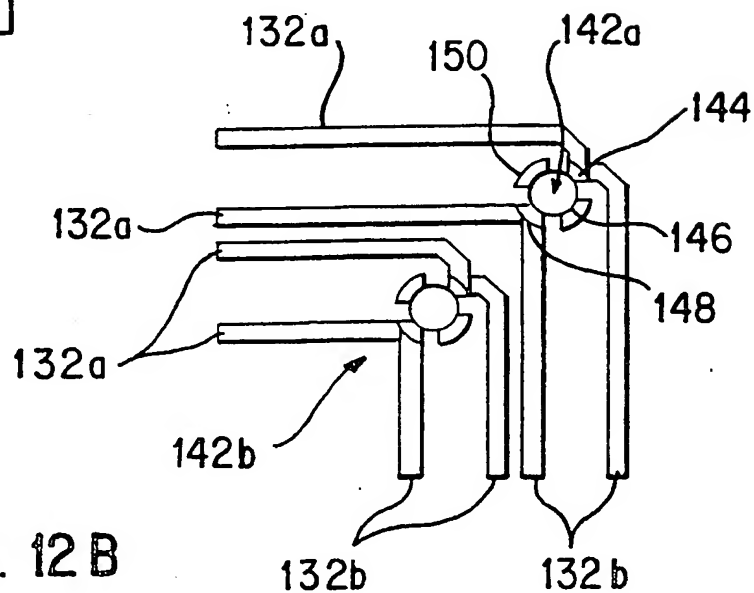


FIG. 12B

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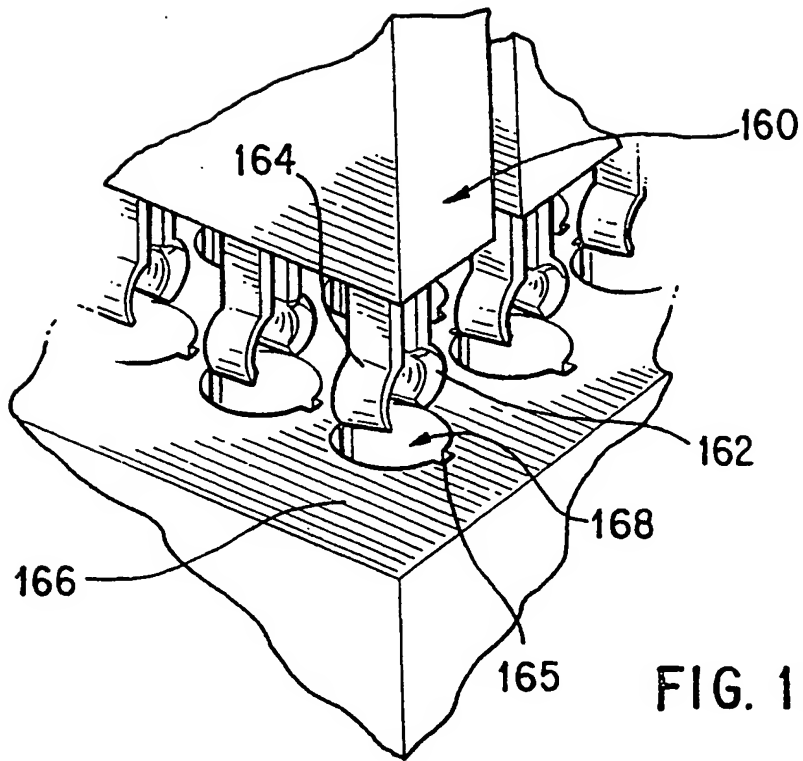


FIG. 13

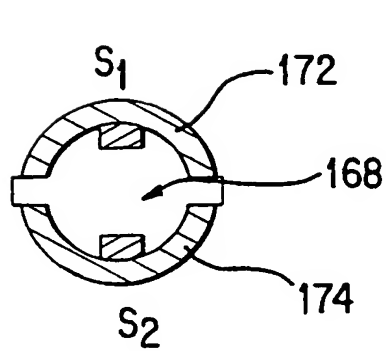


FIG. 13A

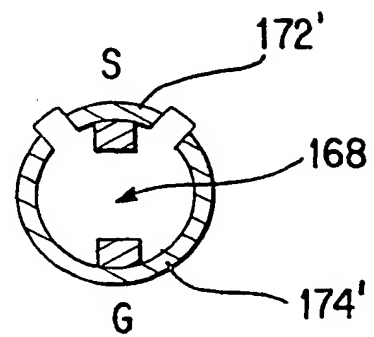


FIG. 13B

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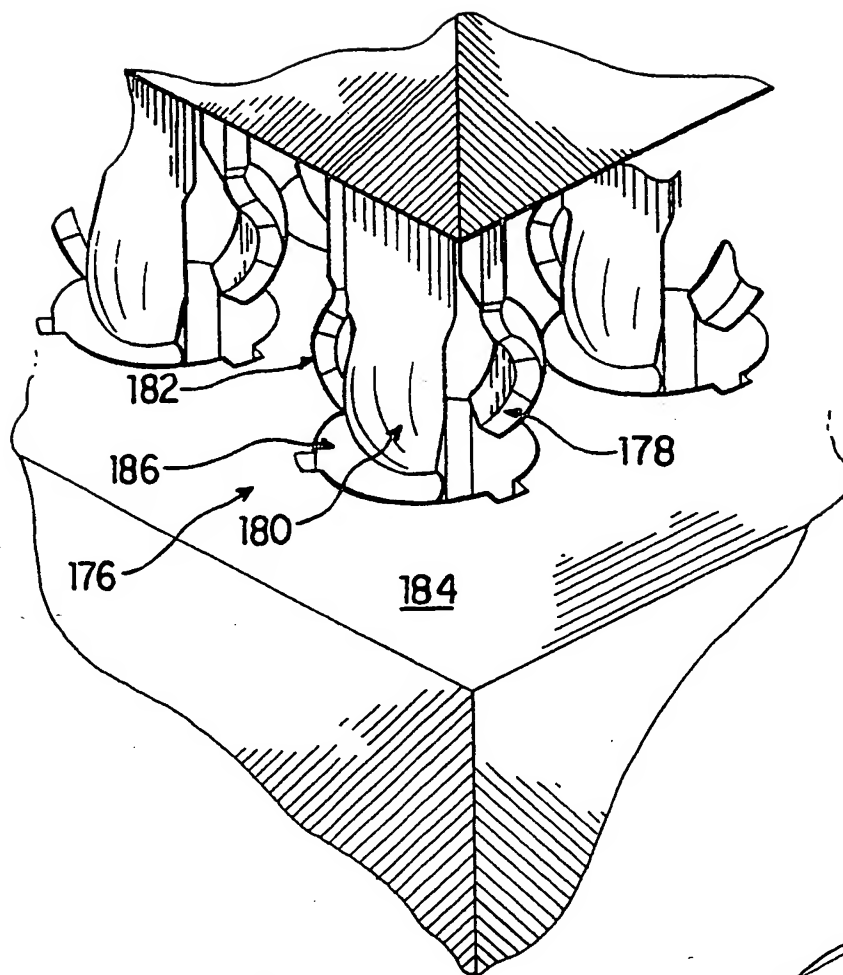


FIG. 13C

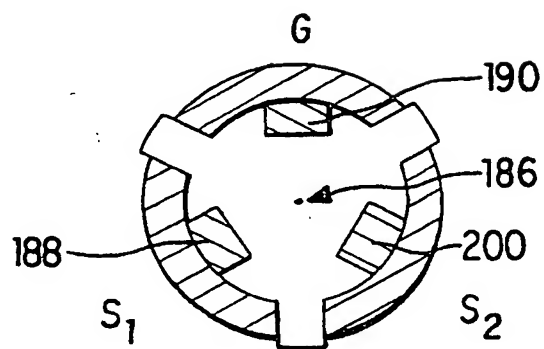


FIG. 13D

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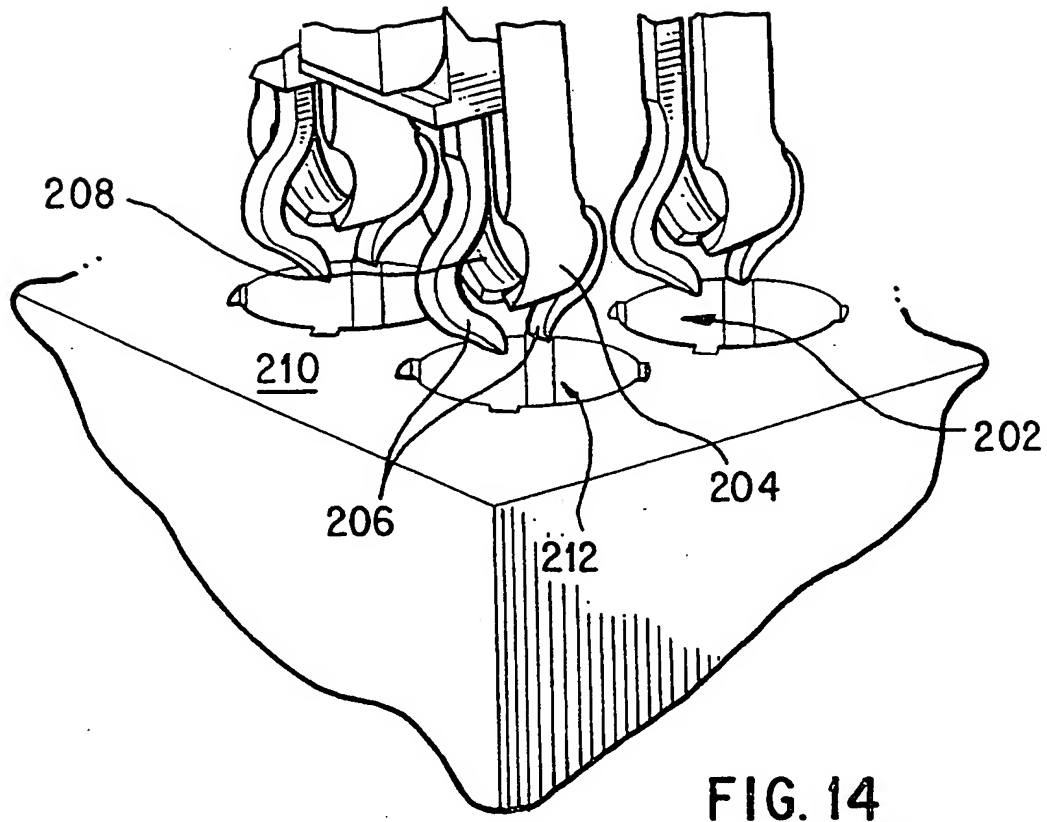


FIG. 14

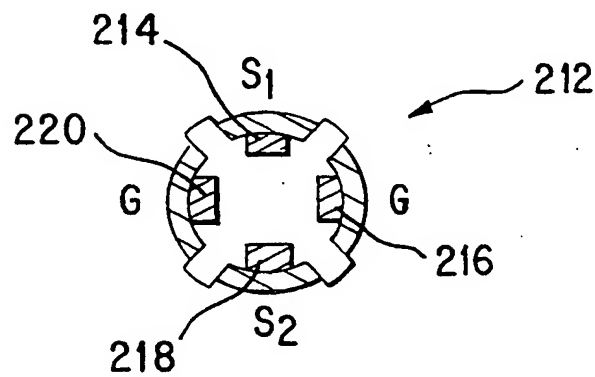


FIG. 14A

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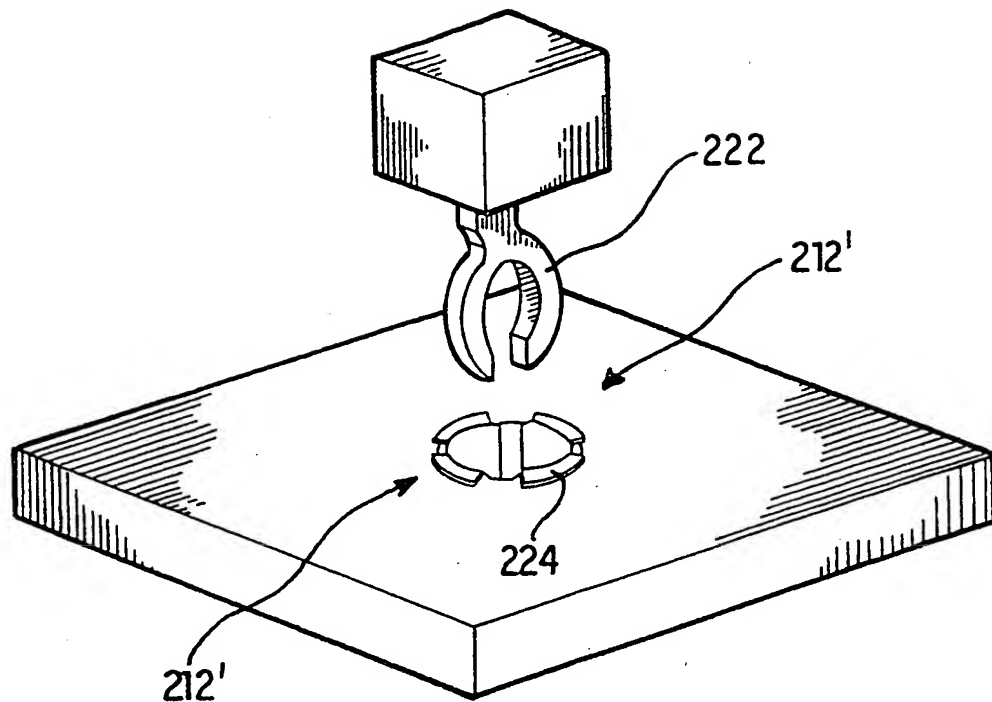


FIG. 15

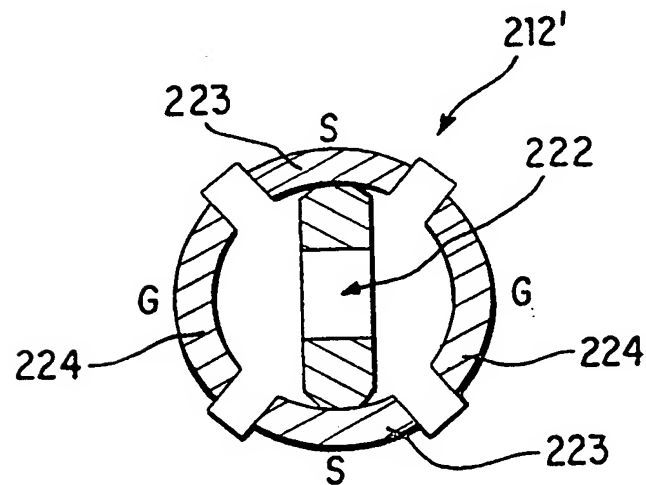


FIG. 15A

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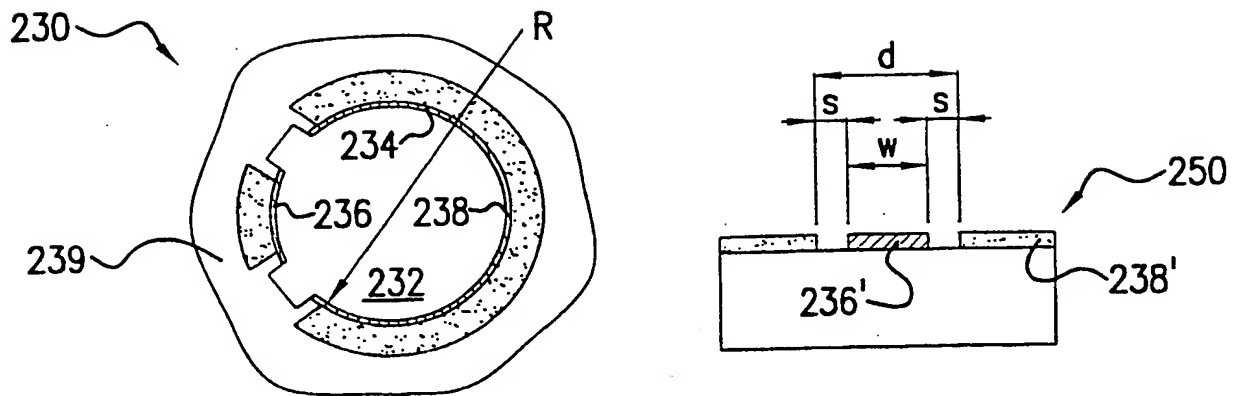


FIG. 16

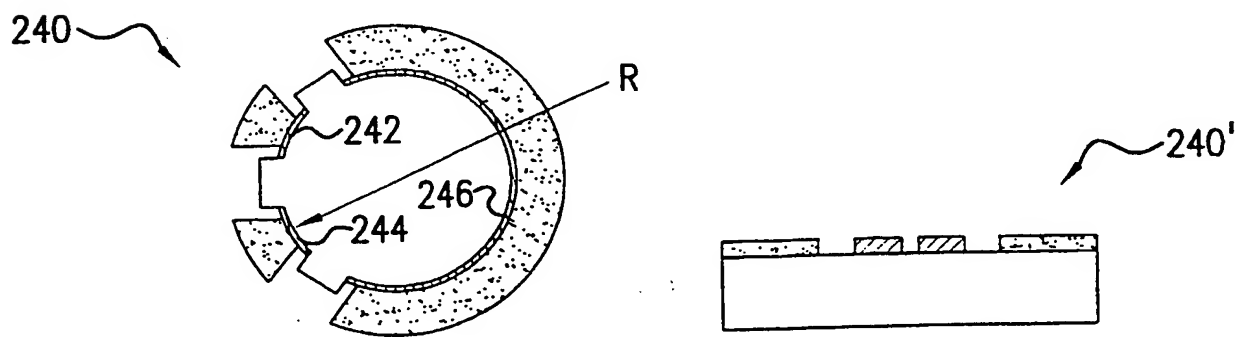


FIG. 17

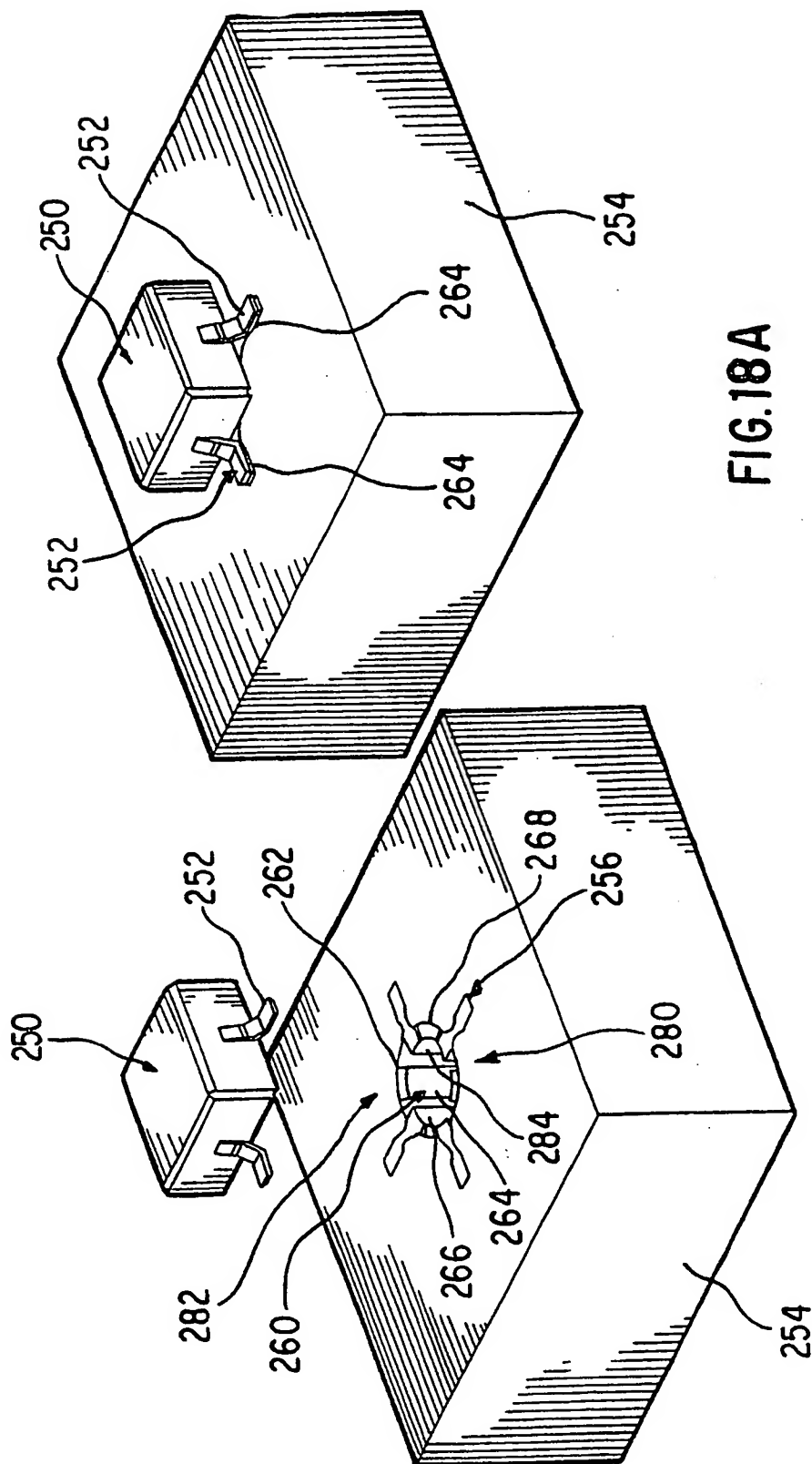


FIG.18A

FIG.18

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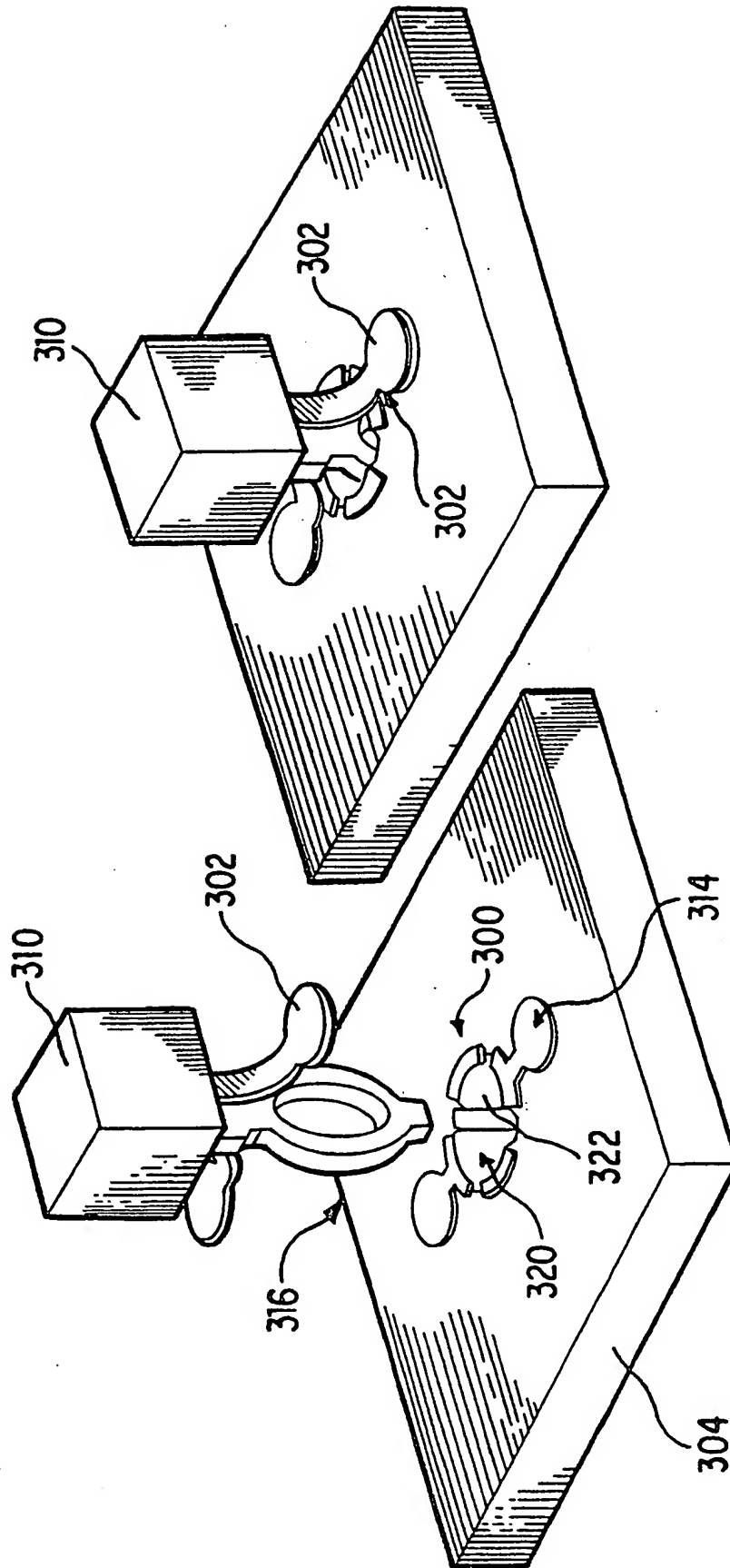


FIG. 19A

FIG. 19

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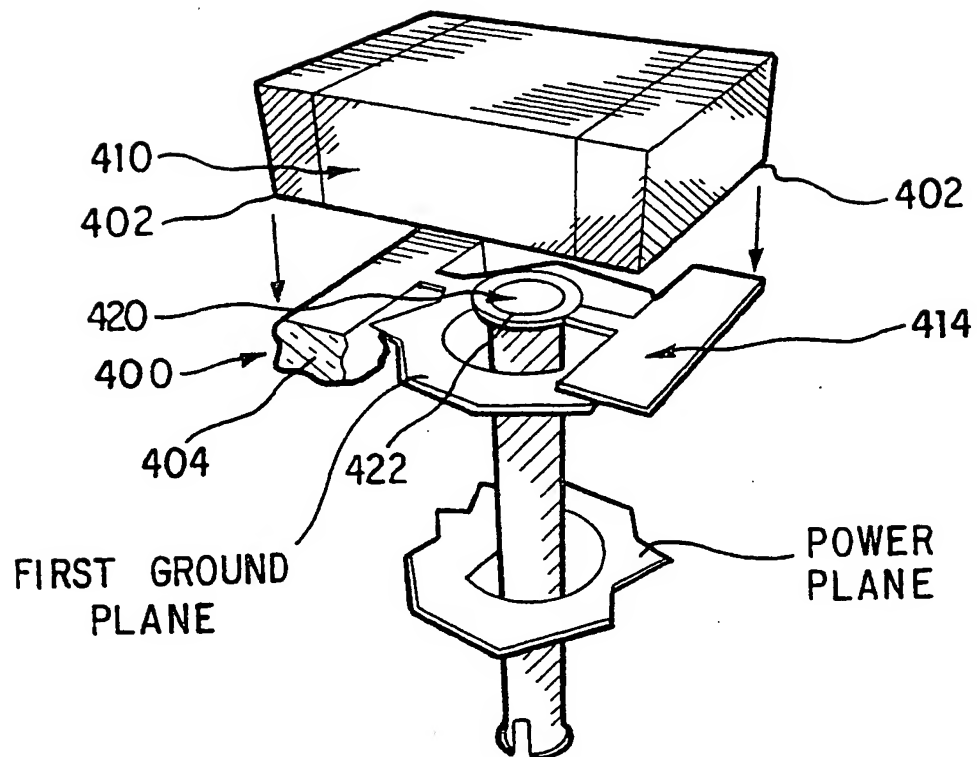


FIG. 20

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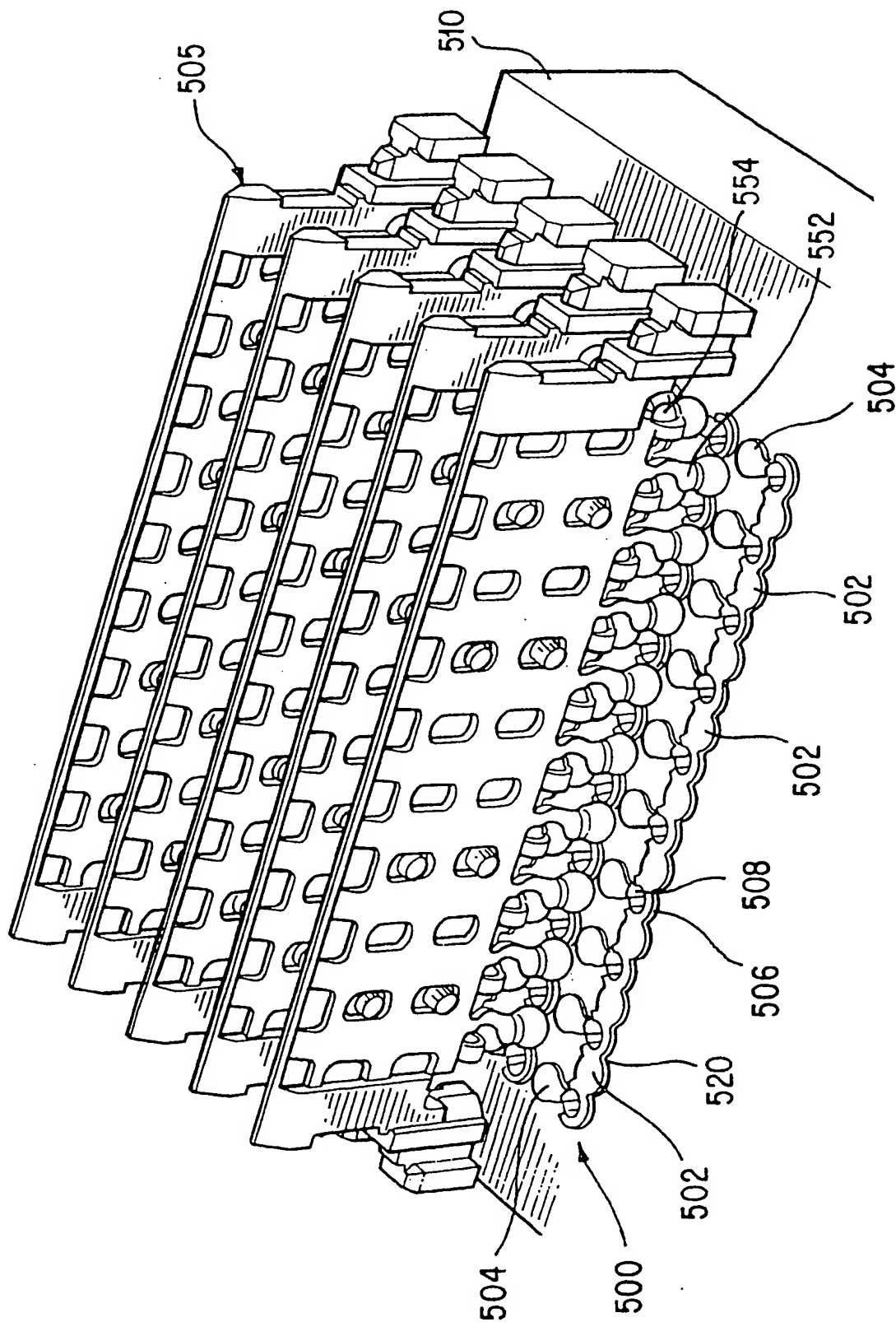
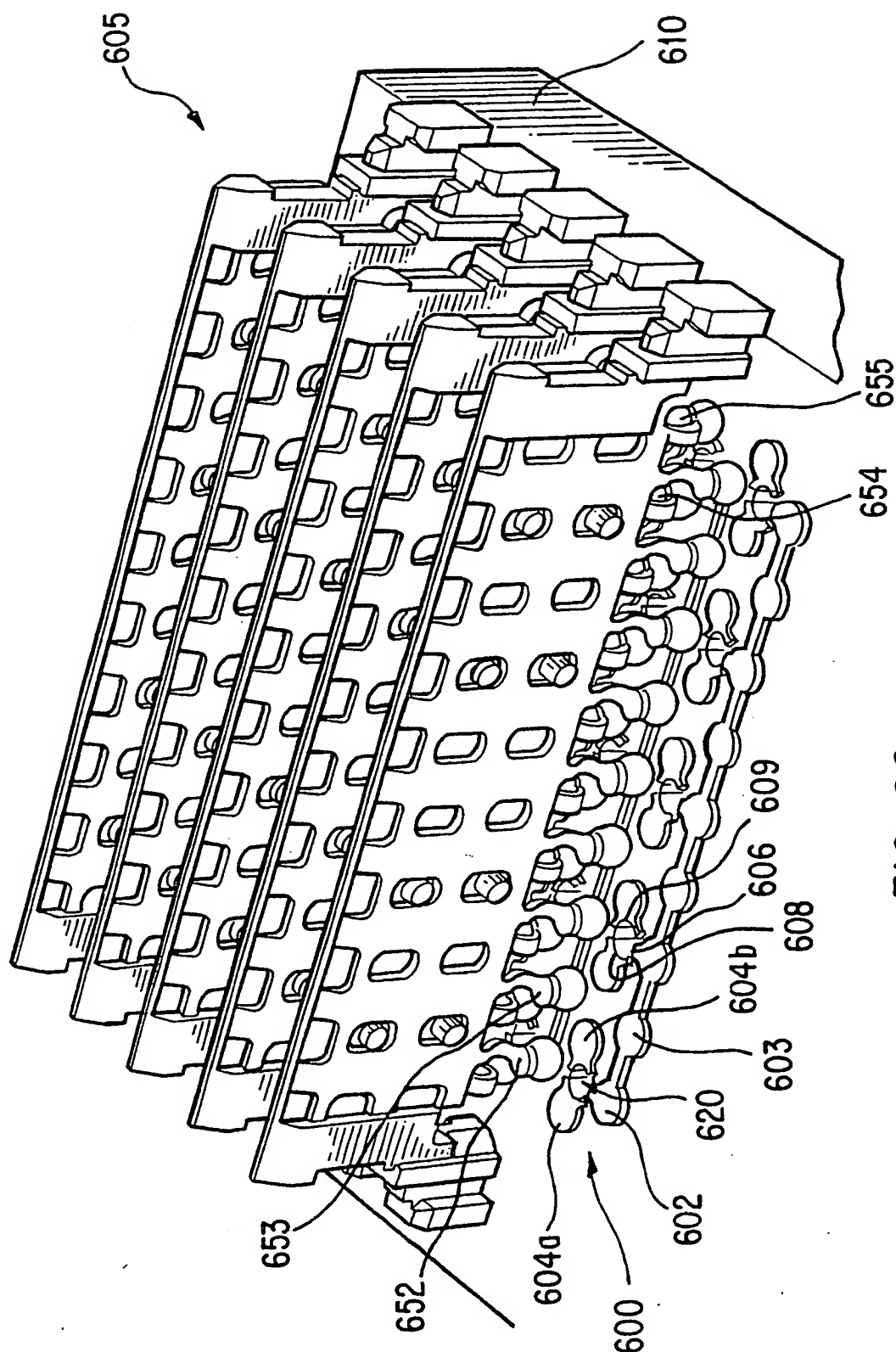


FIG. 21

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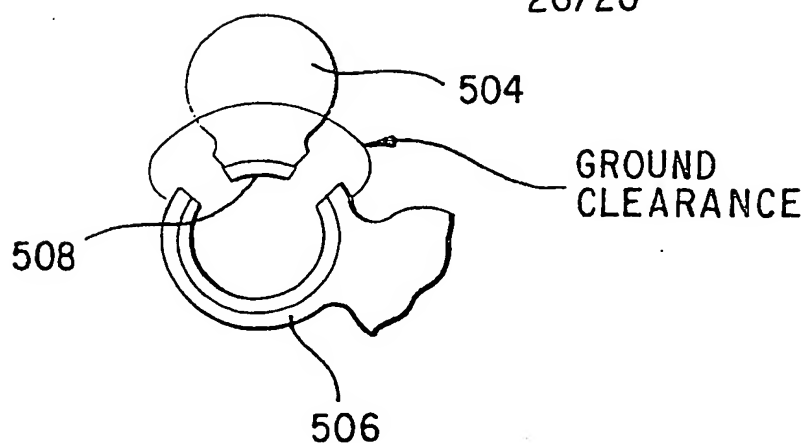


FIG. 21A

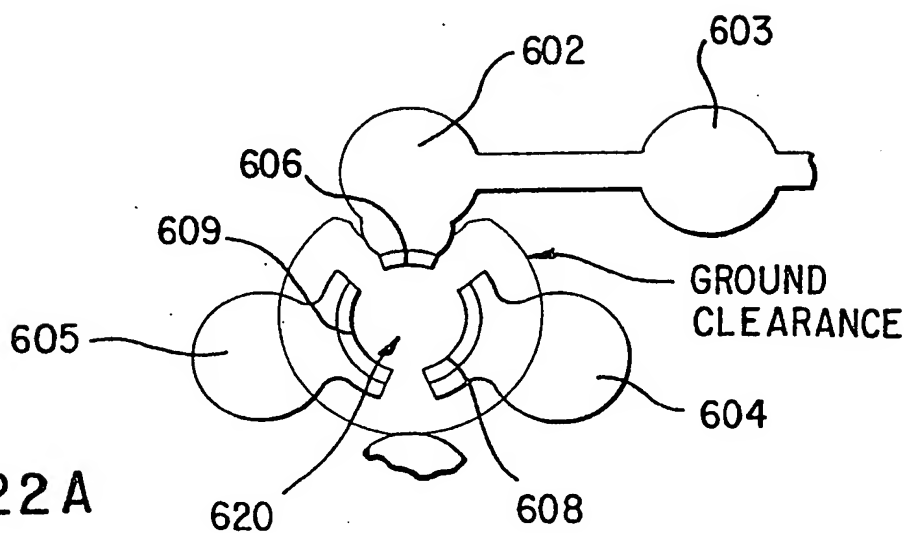


FIG. 22A

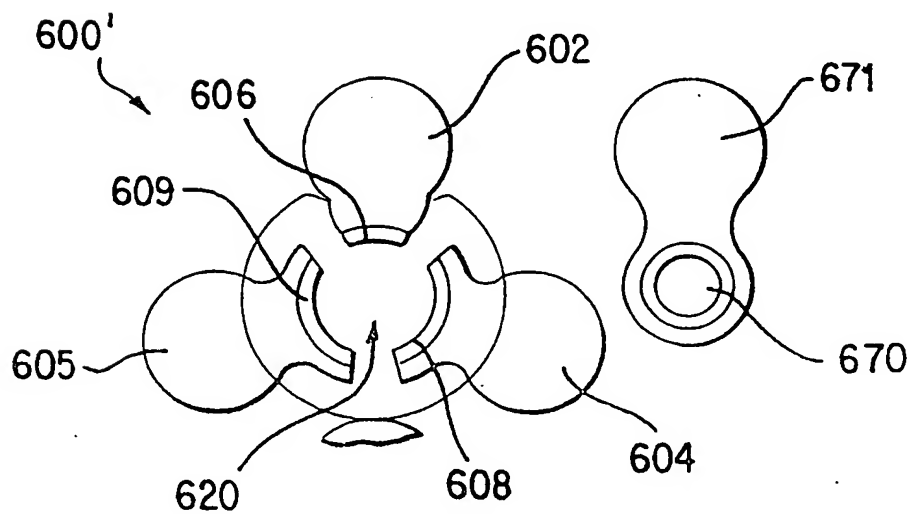


FIG. 23

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